TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

16 GBIT (2G × 8 BIT) CMOS NAND E^{2}PROM

DESCRIPTION

The TH58NVG4S0D is a single 3.3 V 16 Gbits (18,094,227,456 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^{2}PROM) organized as (4096 + 218) bytes × 64 pages × 8192 blocks. The device has four 4314-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 4314-byte increments. The Erase operation is implemented in a single block unit (256 Kbytes + 13.6 Kbytes: 4314 bytes × 64 pages).

The device is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- Organization

	TH58NVG4S0D
Memory cell array	4314 × 256K × 8
Register	4314 × 8
Page size	4314 bytes
Block size	(256K + 13.6K) bytes

- Modes
  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy,
  Multi Page Program, Multi Block Erase, Multi Page Copy, Multi Page Read

- Mode control
  Serial input/output
  Command control

- Number of valid blocks
  Min 8032 blocks
  Max 8192 blocks

- Power supply
  V_{CC} = 2.7 V to 3.6 V

- Access time

Cell array to register	25 μs max
Serial Read Cycle	30 ns min

- Program/Erase time

Auto Page Program	300 μs/page typ.
Auto Block Erase	2 ms/block typ.

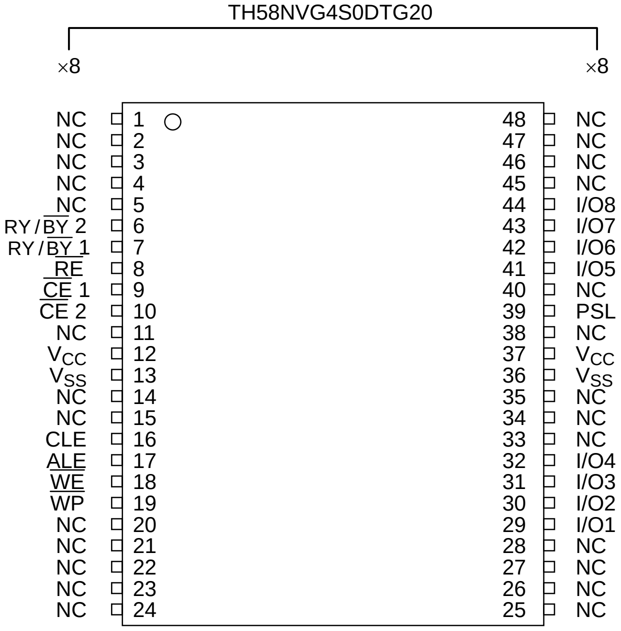
- Operating current

Read (30 ns cycle)	30 mA max.
Program (avg.)	30 mA max.
Erase (avg.)	30 mA max.
Standby	100 μA max

- Package
  TSOP I 48-P-1220-0.50 (Weight: 0.53 g typ.)

- FOR RELIABILITY GUIDANCE, PLEASE REFER TO THE APPLICATION NOTES AND COMMENTS (15).
  1 bit ECC for each 512 bytes is required.

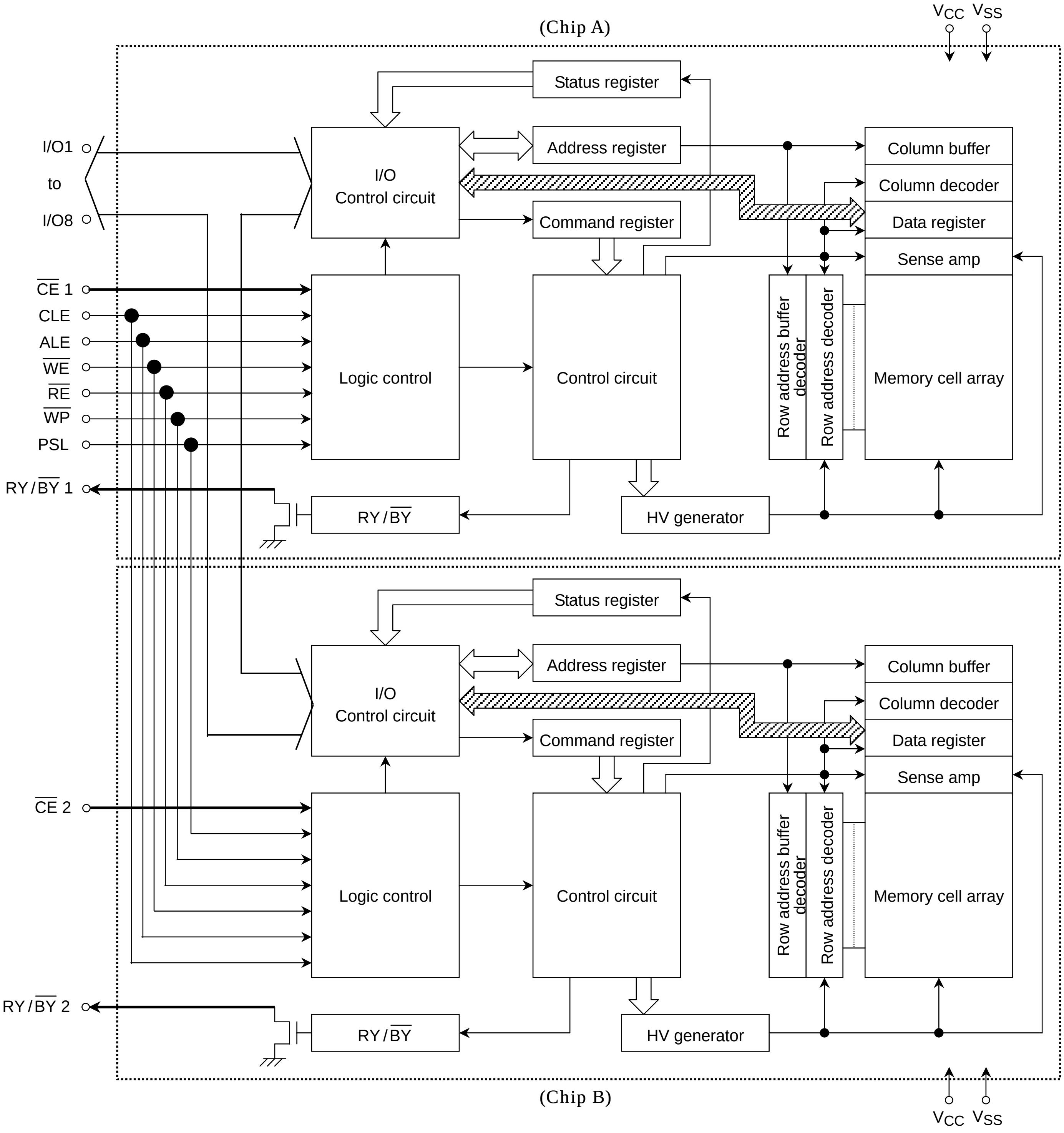
PIN ASSIGNMENT (TOP VIEW)



PINNAMES

I/O1 to I/O8	I/O port
$\overline{\text{CE}}$ 1	Chip enable (Chip A)
$\overline{\text{CE}}$ 2	Chip enable (Chip B)
$\overline{\text{WE}}$	Write enable
$\overline{\text{RE}}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
PSL	Power on select
$\overline{\text{WP}}$	Write protect
RY/$\overline{\text{BY}}$ 1	Ready/Busy (Chip A)
RY/$\overline{\text{BY}}$ 2	Ready/Busy (Chip B)
V_{CC}	Power supply
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input /Output Voltage	−0.6 V to V_{CC} + 0.3 V (≤ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	−55 to 150	°C
T_{OPR}	Operating Temperature	0 to 70	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	20	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	20	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	8032	—	8192	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (12) toward the end of this document.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over the device lifetime.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER		MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage		2.7 V	—	3.6 V	V
V_{IH}	High Level input Voltage	$2.7\ V \le V_{CC} \le 3.6\ V$	0.78 x Vcc	—	$V_{CC} + 0.3$	V
V_{IL}	Low Level Input Voltage	$2.7\ V \le V_{CC} \le 3.6\ V$	−0.3*	—	0.22 x Vcc	V

* −2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0\ V$ to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0\ V$ to V_{CC}	—	—	±10	μA
I_{CCO0}*	Power On Reset Current	PSL = GND or NU	—	—	30	mA
		PSL = V_{CC}, FFh command input after Power On	—	—	30	
I_{CCO1}	Serial Read Current	$\overline{CE} = V_{IL}$, $I_{OUT} = 0$ mA, tcycle = 30 ns	—	—	30	mA
I_{CCO2}	Programming Current	—	—	—	30	mA
I_{CCO3}	Erasing Current	—	—	—	30	mA
I_{CCS}	Standby Current	$\overline{CE} = V_{CC} - 0.2\ V$, $\overline{WP} = 0\ V/V_{CC}$, PSL = 0 V/$V_{CC}$/NU	—	—	100	μA
V_{OH}	High Level Output Voltage	$I_{OH} = -0.4$ mA ($2.7\ V \le V_{CC} \le 3.6\ V$)	2.4	—	—	V
V_{OL}	Low Level Output Voltage	$I_{OL} = 2.1$ mA ($2.7\ V \le V_{CC} \le 3.6\ V$)	—	—	0.4	V
I_{OL} (RY/$\overline{BY}$)	Output current of RY/$\overline{BY}$ pin	$V_{OL} = 0.4\ V$ ($2.7\ V \le V_{CC} \le 3.6\ V$)	—	8	—	mA

* Refer to application note (2) for detail

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS
(Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CLS}	CLE Setup Time	0	—	ns
t_{CLS2}	CLE Setup Time	30	—	ns
t_{CLH}	CLE Hold Time	6	—	ns
t_{CS}	$\overline{\text{CE}}$ Setup Time	10	—	ns
t_{CS2}	$\overline{\text{CE}}$ Setup Time	20	—	ns
t_{CH}	$\overline{\text{CE}}$ Hold Time	6	—	ns
t_{WP}	Write Pulse Width	15	—	ns
t_{ALS}	ALE Setup Time	0	—	ns
t_{ALH}	ALE Hold Time	6	—	ns
t_{DS}	Data Setup Time	10	—	ns
t_{DH}	Data Hold Time	5	—	ns
t_{WC}	Write Cycle Time	30	—	ns
t_{WH}	$\overline{\text{WE}}$ High Hold Time	10	—	ns
t_{WHW} *	$\overline{\text{WE}}$ High Hold Time from final address to first data	40	—	ns
t_{WW}	$\overline{\text{WP}}$ High to $\overline{\text{WE}}$ Low	100	—	ns
t_{RR}	Ready to $\overline{\text{RE}}$ Falling Edge	20	—	ns
t_{RW}	Ready to $\overline{\text{WE}}$ Falling Edge	20	—	ns
t_{RP}	Read Pulse Width	15	—	ns
t_{RC}	Read Cycle Time	30	—	ns
t_{REA}	$\overline{\text{RE}}$ Access Time	—	25	ns
t_{CR}	$\overline{\text{CE}}$ Low to $\overline{\text{RE}}$ Low	10	—	ns
t_{CLR}	CLE Low to $\overline{\text{RE}}$ Low	10	—	ns
t_{AR}	ALE Low to $\overline{\text{RE}}$ Low	10	—	ns
t_{RHOH}	Data Output Hold Time from $\overline{\text{RE}}$ High	30	—	ns
t_{RLOH}	Data Output Hold Time from $\overline{\text{RE}}$ Low	5	—	ns
t_{RHZ}	$\overline{\text{RE}}$ High to Output High Impedance	—	60	ns
t_{CHZ}	$\overline{\text{CE}}$ High to Output High Impedance	—	30	ns
t_{CLHZ}	CLE High to Output High Impedance	—	30	ns
t_{REH}	$\overline{\text{RE}}$ High Hold Time	15	—	ns
t_{IR}	Output-High-impedance-to-$\overline{\text{RE}}$ Falling Edge	0	—	ns
t_{RHW}	$\overline{\text{RE}}$ High to $\overline{\text{WE}}$ Low	30	—	ns
t_{WHC}	$\overline{\text{WE}}$ High to $\overline{\text{CE}}$ Low	30	—	ns
t_{WHR}	$\overline{\text{WE}}$ High to $\overline{\text{RE}}$ Low	100	—	ns
t_{R}	Memory Cell Array to Starting Address	—	25	µs
$t_{DCBSYR1}$	Data Cache Busy in Read Cache (following 31h and 3Fh)	—	25	µs
$t_{DCBSYR2}$	Data Cache Busy in Page Copy (following 3Ah)	—	30	µs

t_{WB}	$\overline{WE}$ High to Busy	—	100	ns
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	—	10/10/30/500	μs

* tWHW is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ falling edge of first data cycle.

AC TEST CONDITIONS

PARAMETER	CONDITION
	2.7 V ≤ V_{CC} ≤ 3.6 V
Input level	0 V to Vcc
Input pulse rise and fall time	5ns
Input comparison level	Vcc/2
Output data comparison level	Vcc/2
Output load	C_L (50 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the RY / $\overline{BY}$ pin.
(Refer to Application Note (9) toward the end of this document.)

PROGRAMMING AND ERASING CHARACTERISTICS
(Ta = 0 to 70°C, V_{CC} = 2.7 V to 3.6 V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time	—	300	500	µs	
$t_{DCBSYW1}$	Data Cache Busy Time in Write Cache (following 11h)	—	—	10	µs	
$t_{DCBSYW2}$	Data Cache Busy Time in Write Cache (following 15h)	—	—	500	µs	(2)
N	Number of Partial Program Cycles in the Same Page	—	—	4		(1)
t_{BERASE}	Block Erasing Time	—	2	10	ms	

(1) A page can be divided into up to 4 segments.Each segment can be programmed individually without an intervning erase operation.

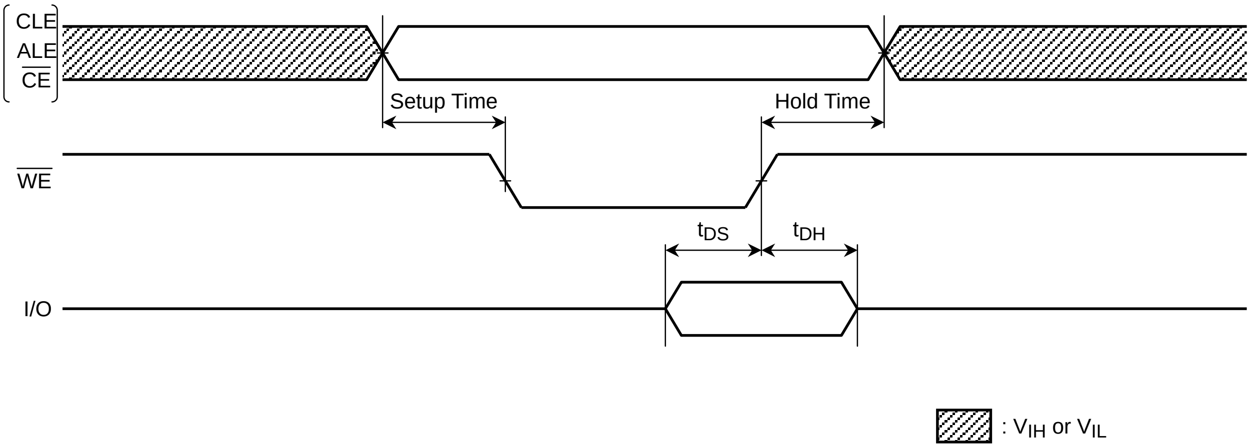
(2) $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.

Data Output

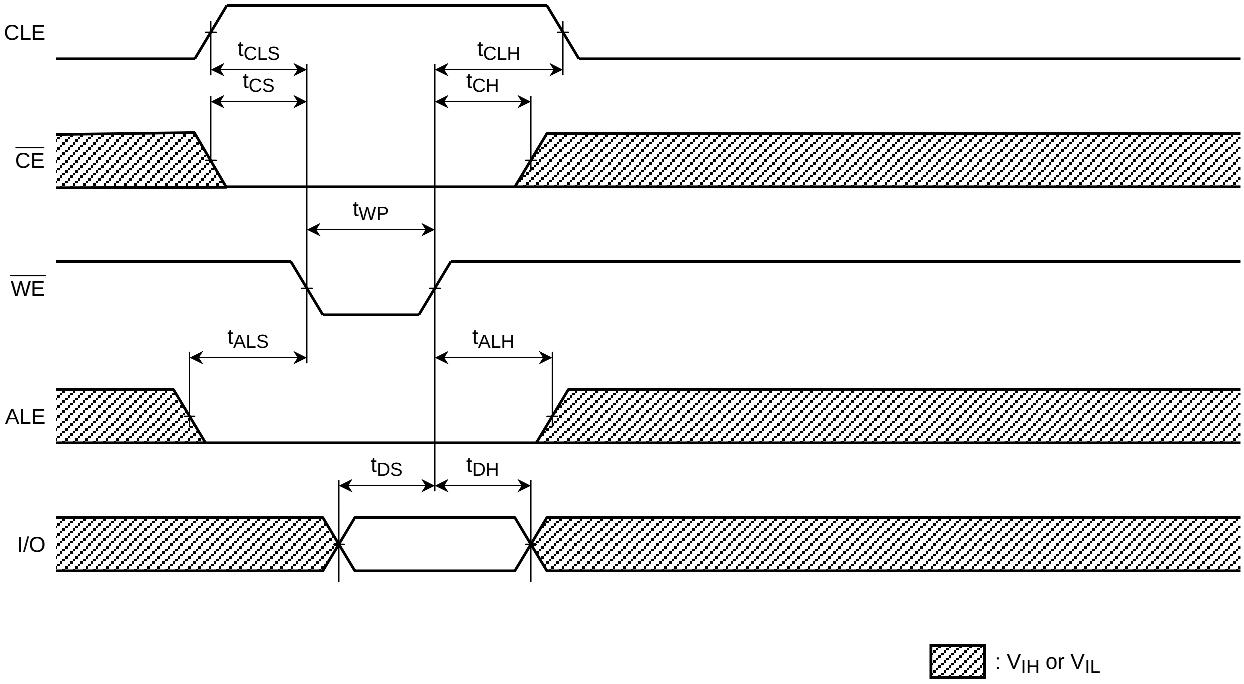
When tREH is long, output buffers are disabled by /RE=High, and the hold time of data output depend on tRHOH (30 ns MIN). On this condition, waveforms look like normal serial read mode.
When tREH is short, output buffers are not disabled by /RE=High, and the hold time of data output depend on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE, ALE, /CE or falling edge of /WE, and waveforms look like Extended Data Output Mode.

TIMING DIAGRAMS

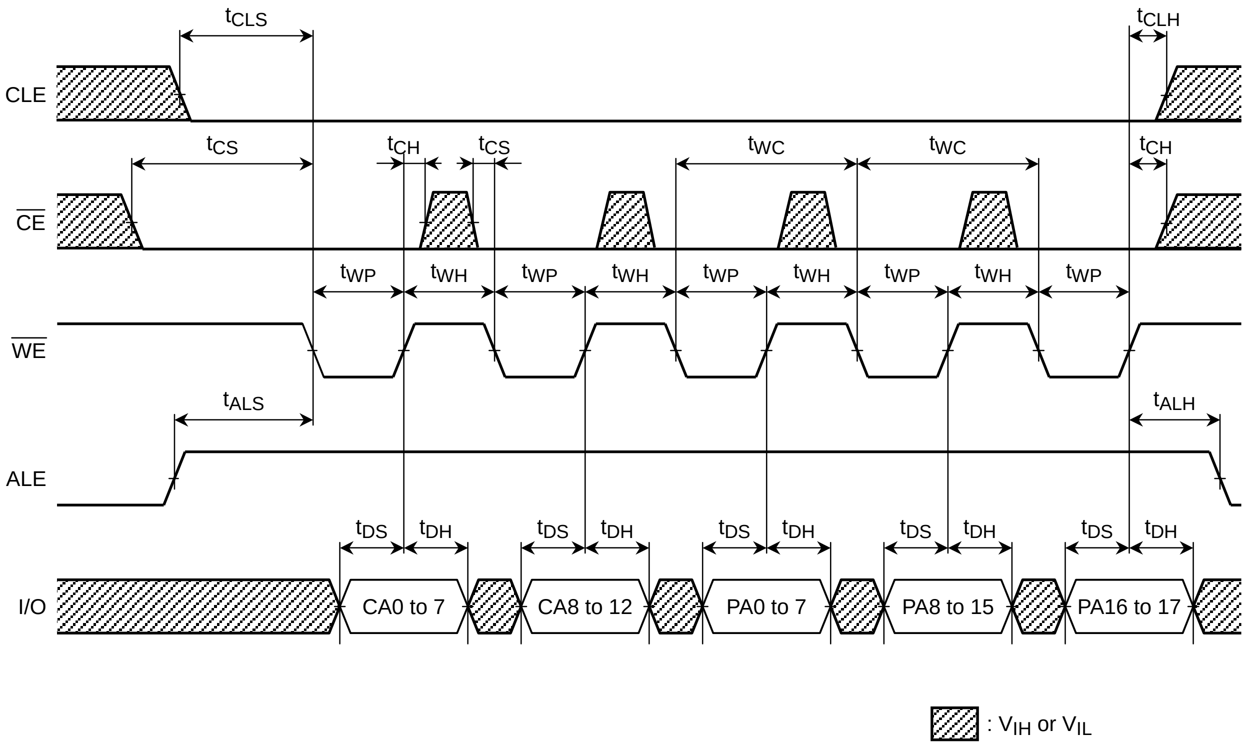
Latch Timing Diagram for Command/Address/Data



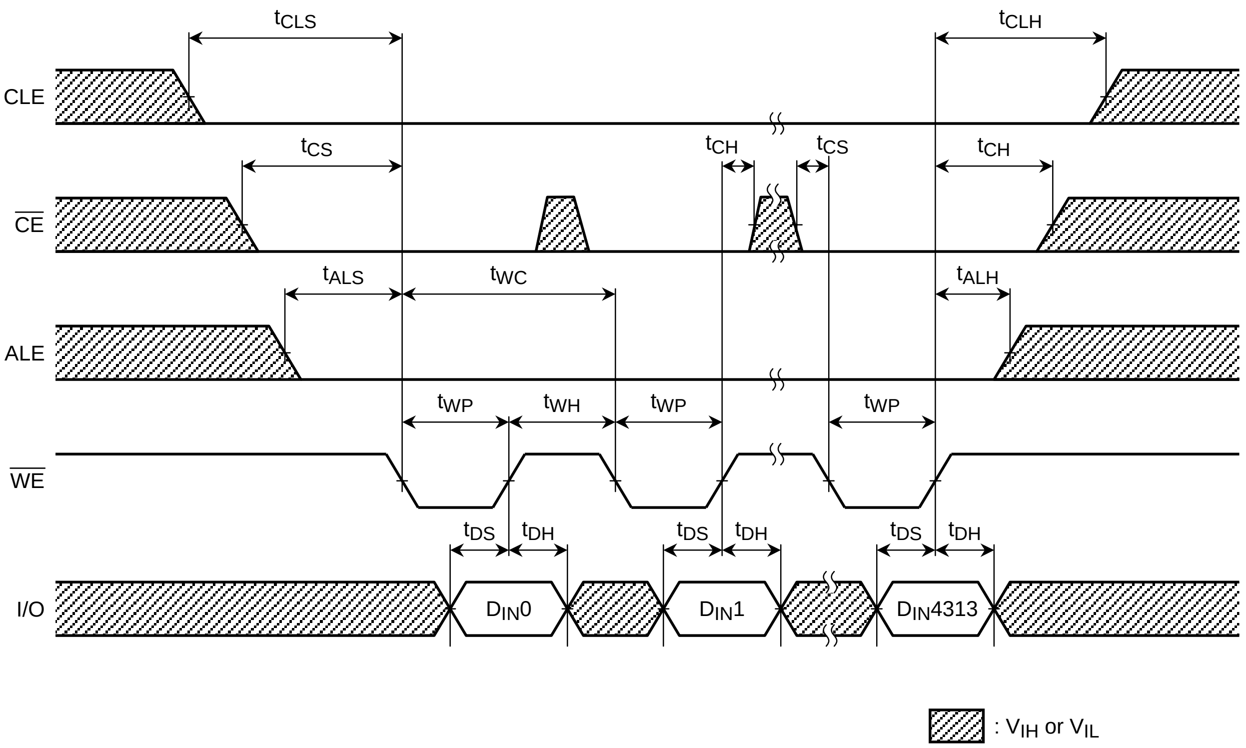
Command Input Cycle Timing Diagram



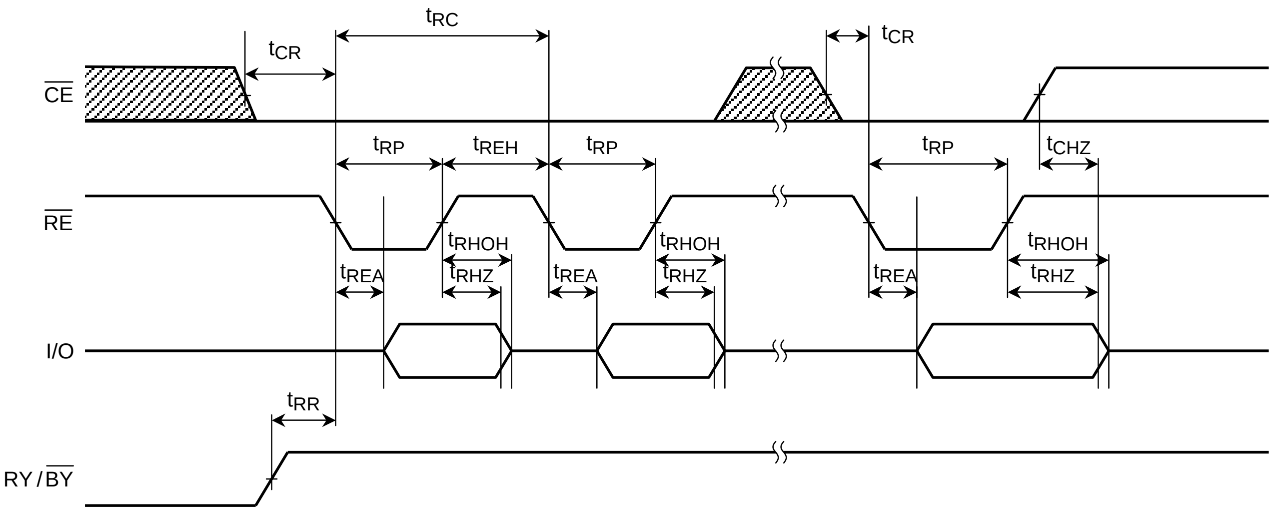
Address Input Cycle Timing Diagram



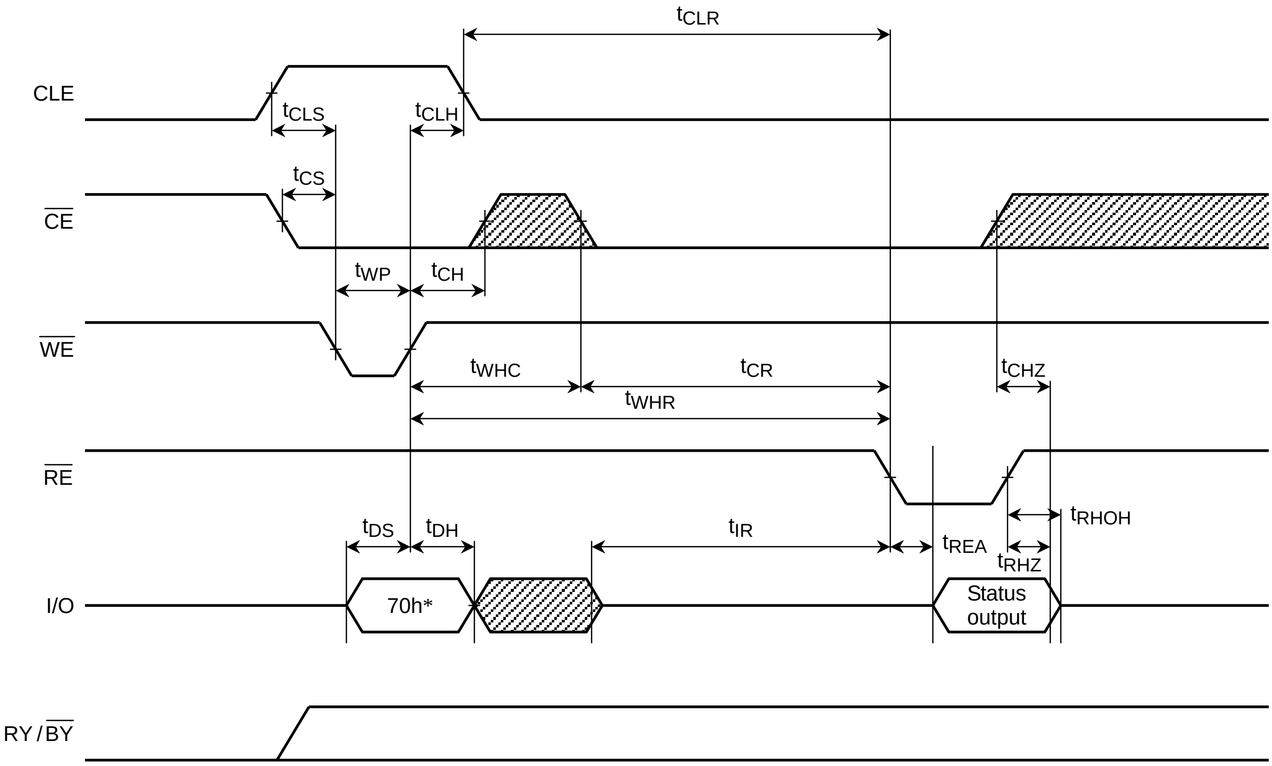
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram



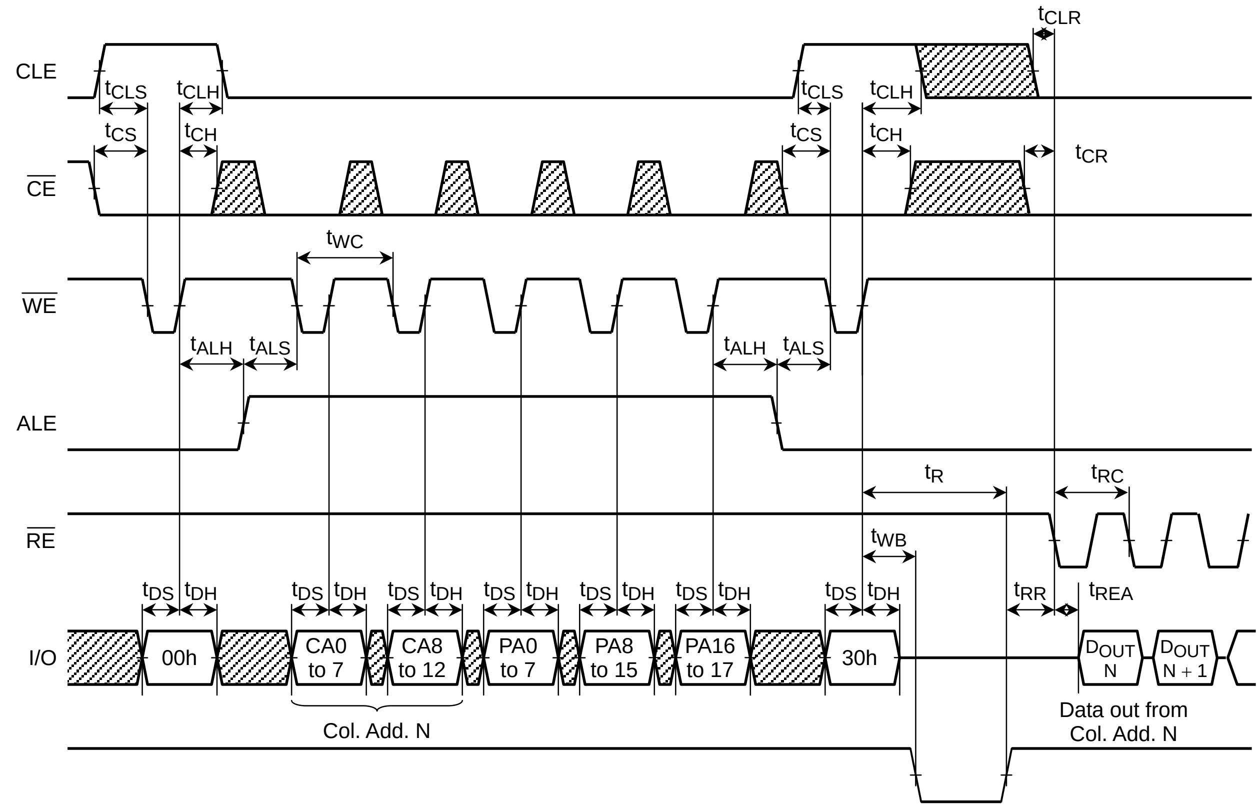
Status Read Cycle Timing Diagram



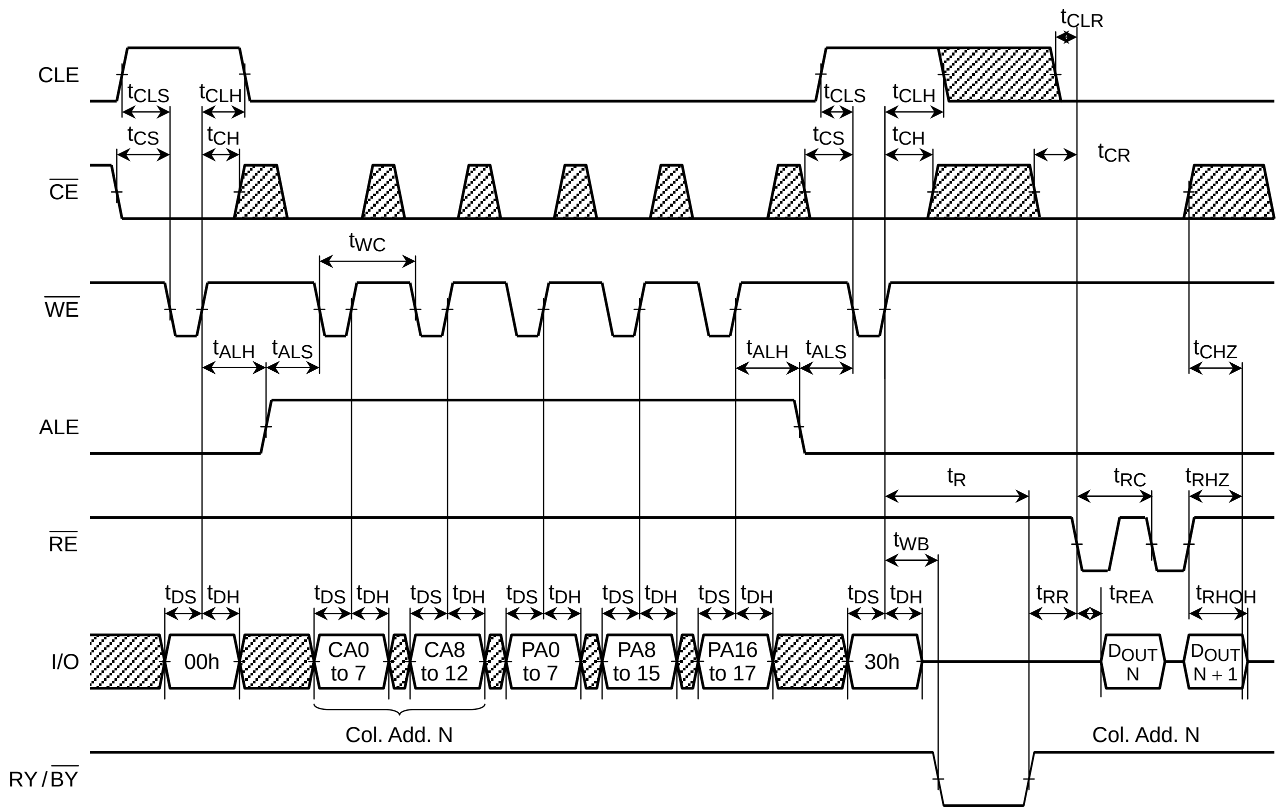
*: 70h represents the hexadecimal number

▨ : V_{IH} or V_{IL}

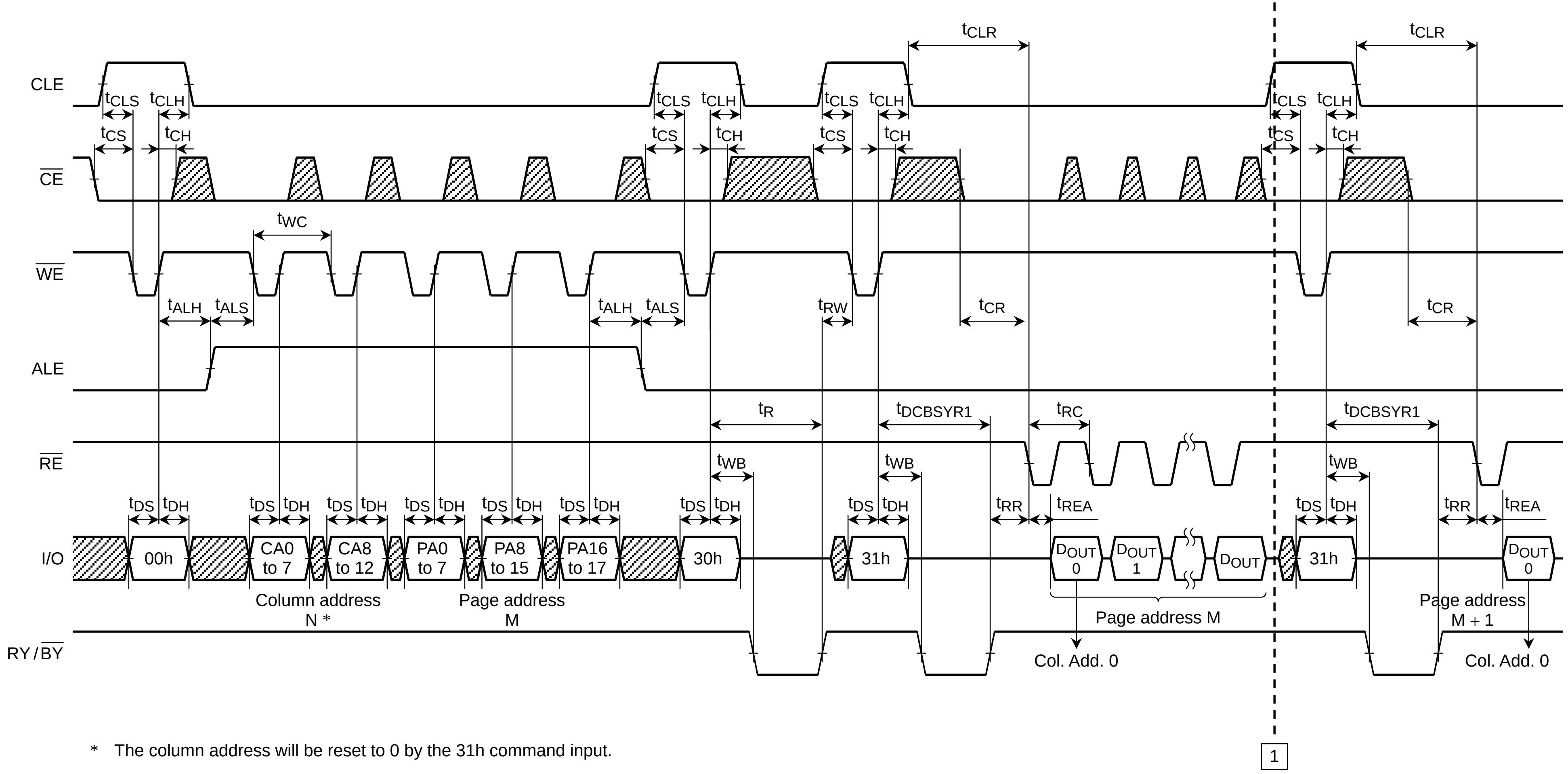
Read Cycle Timing Diagram



Read Cycle Timing Diagram: When Interrupted by CE



Read Cycle with Data Cache Timing Diagram (1/2)



* The column address will be reset to 0 by the 31h command input.

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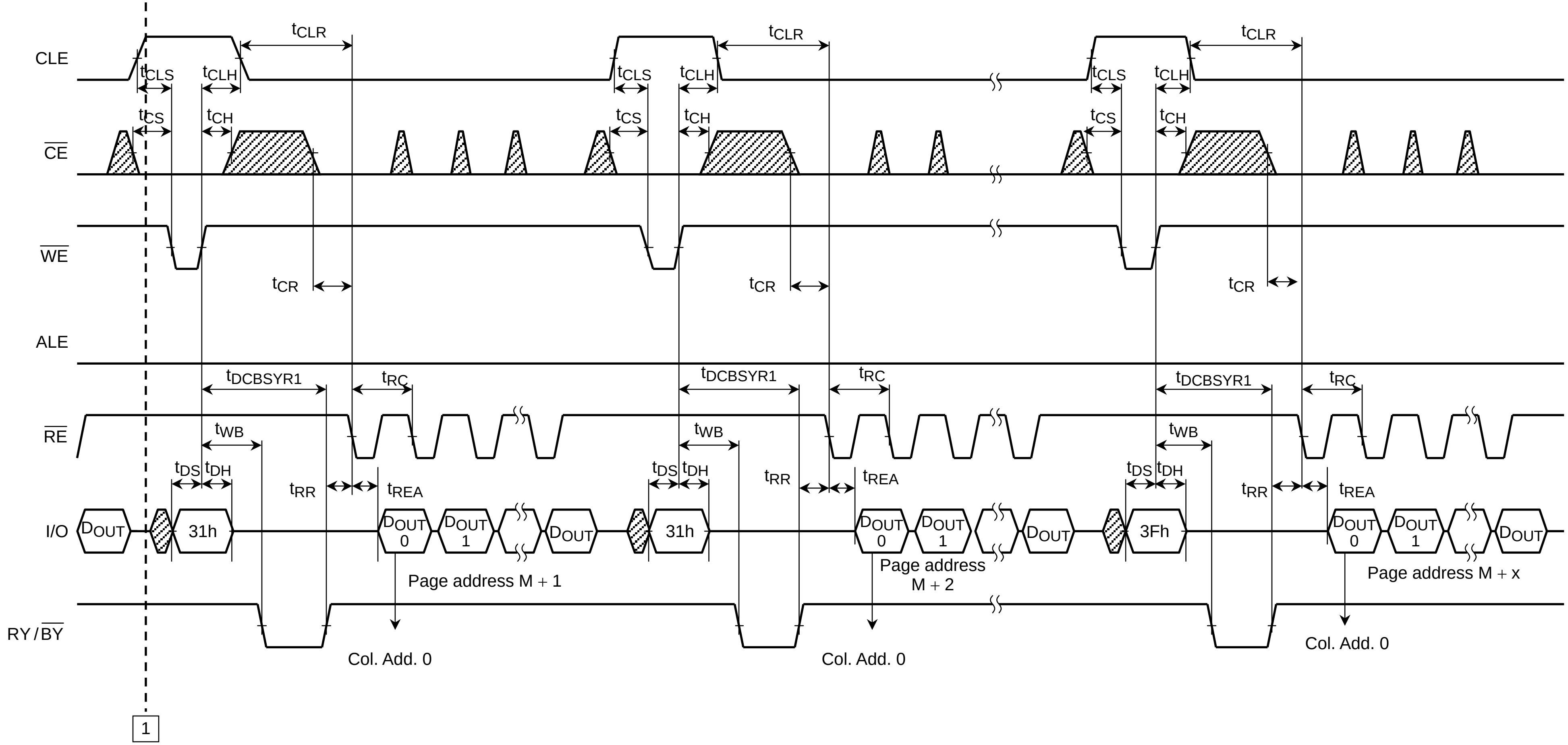
Read Cycle with Data Cache Timing Diagram (2/2)



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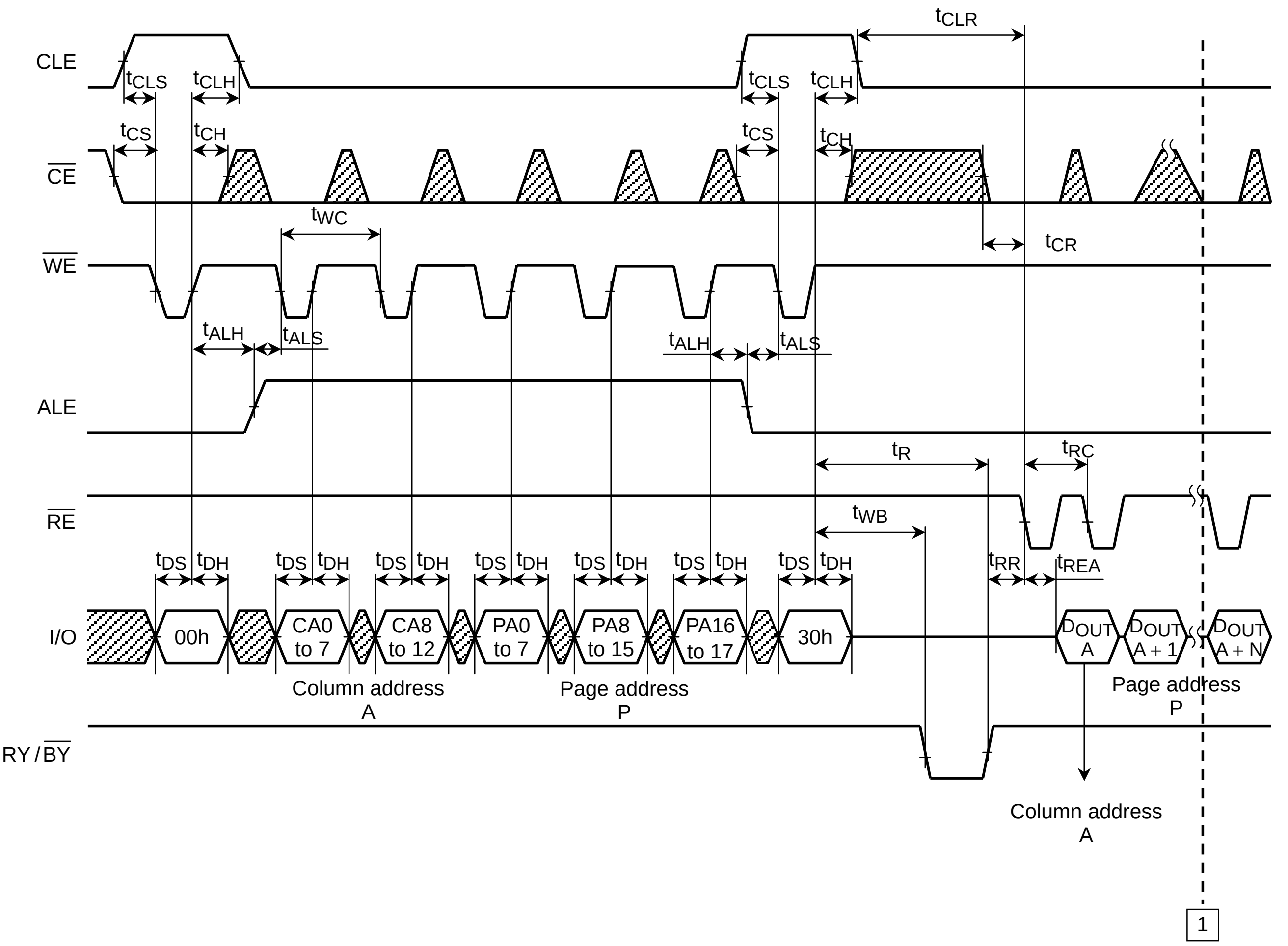
Column Address Change in Read Cycle Timing Diagram (1/2)



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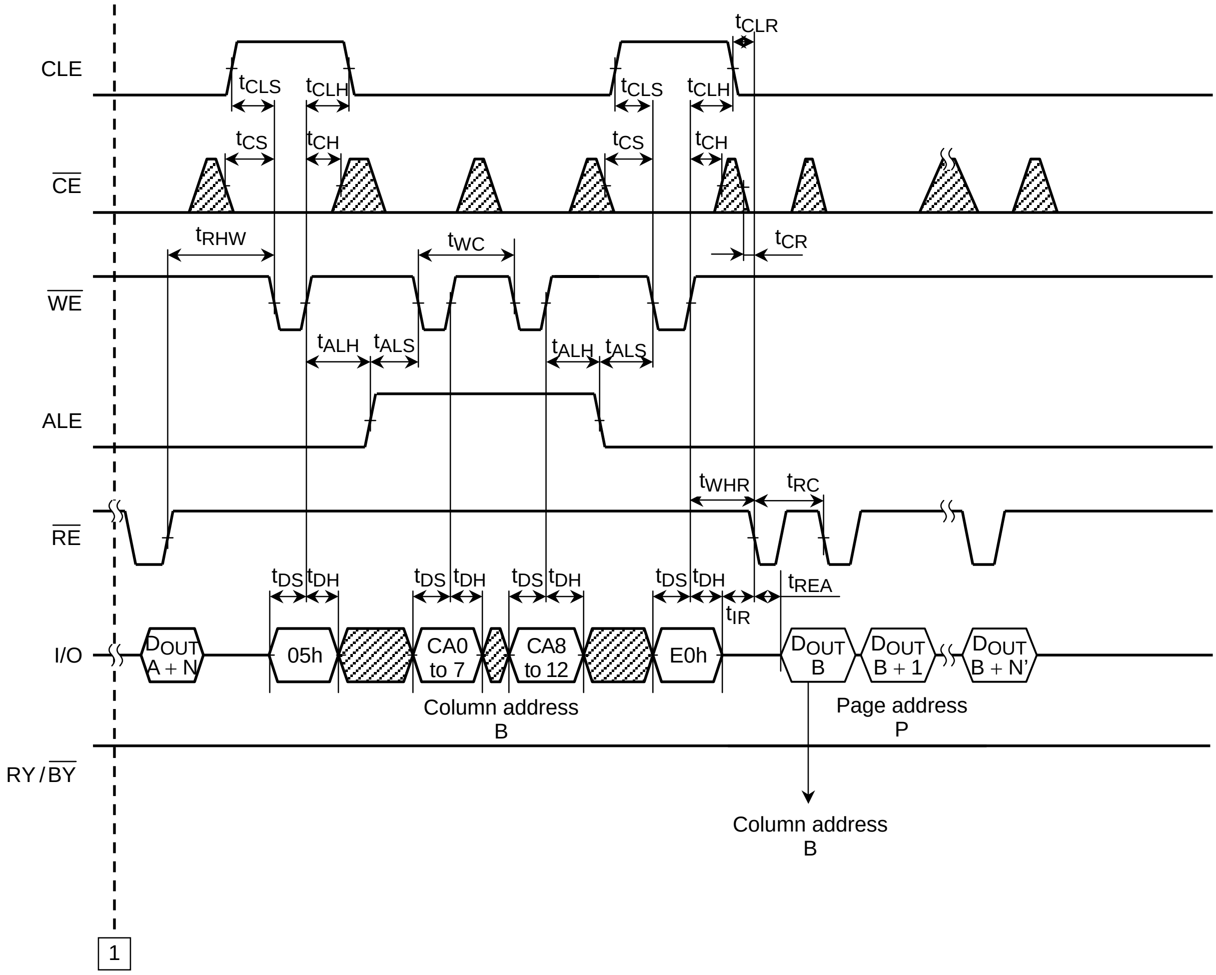
Column Address Change in Read Cycle Timing Diagram (2/2)



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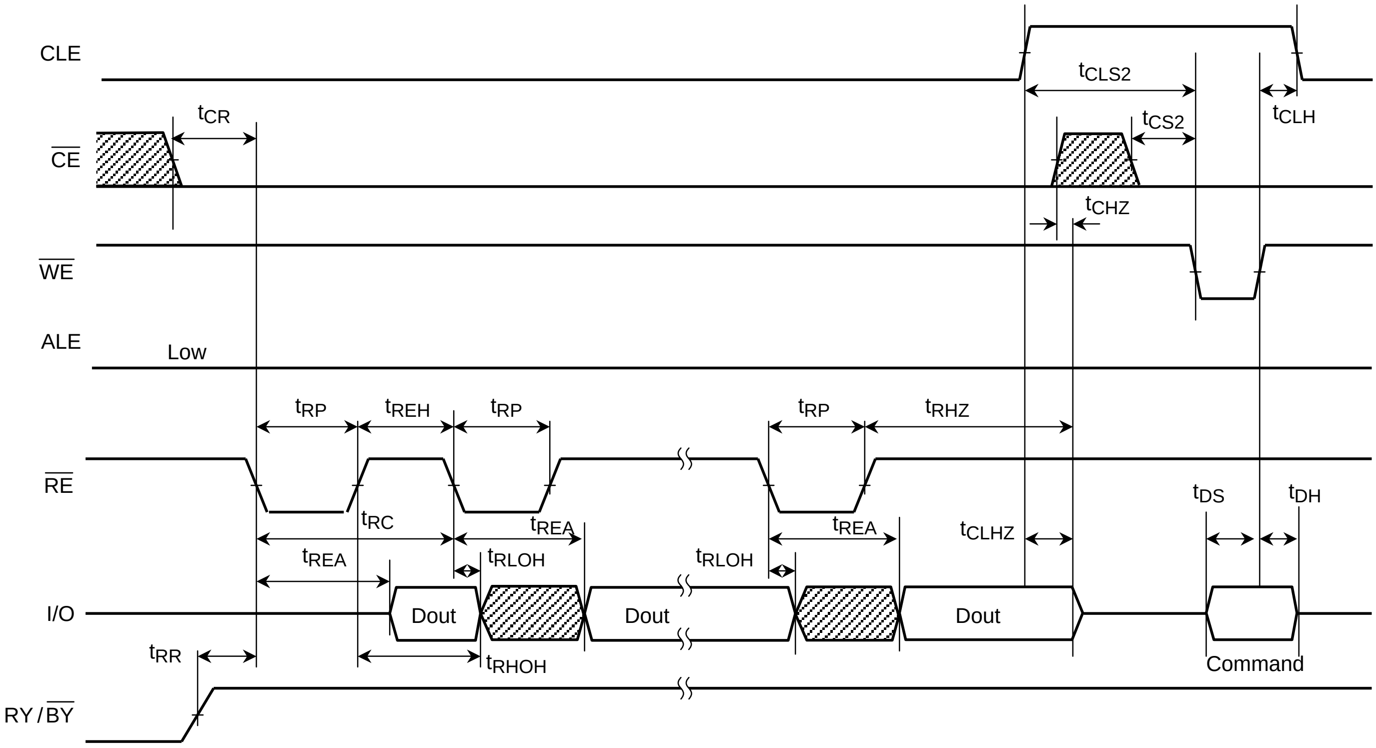
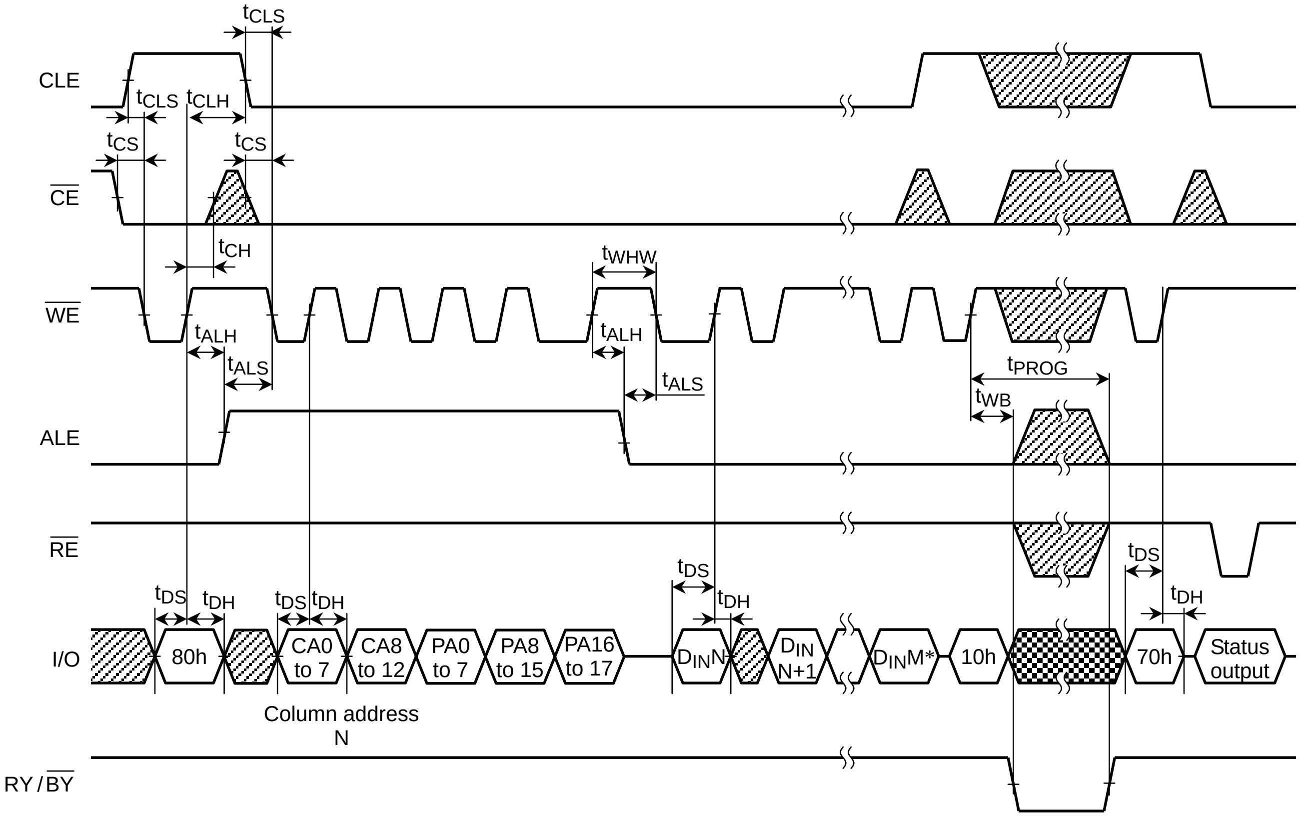
Data Output Timing Diagram



Auto-Program Operation Timing Diagram

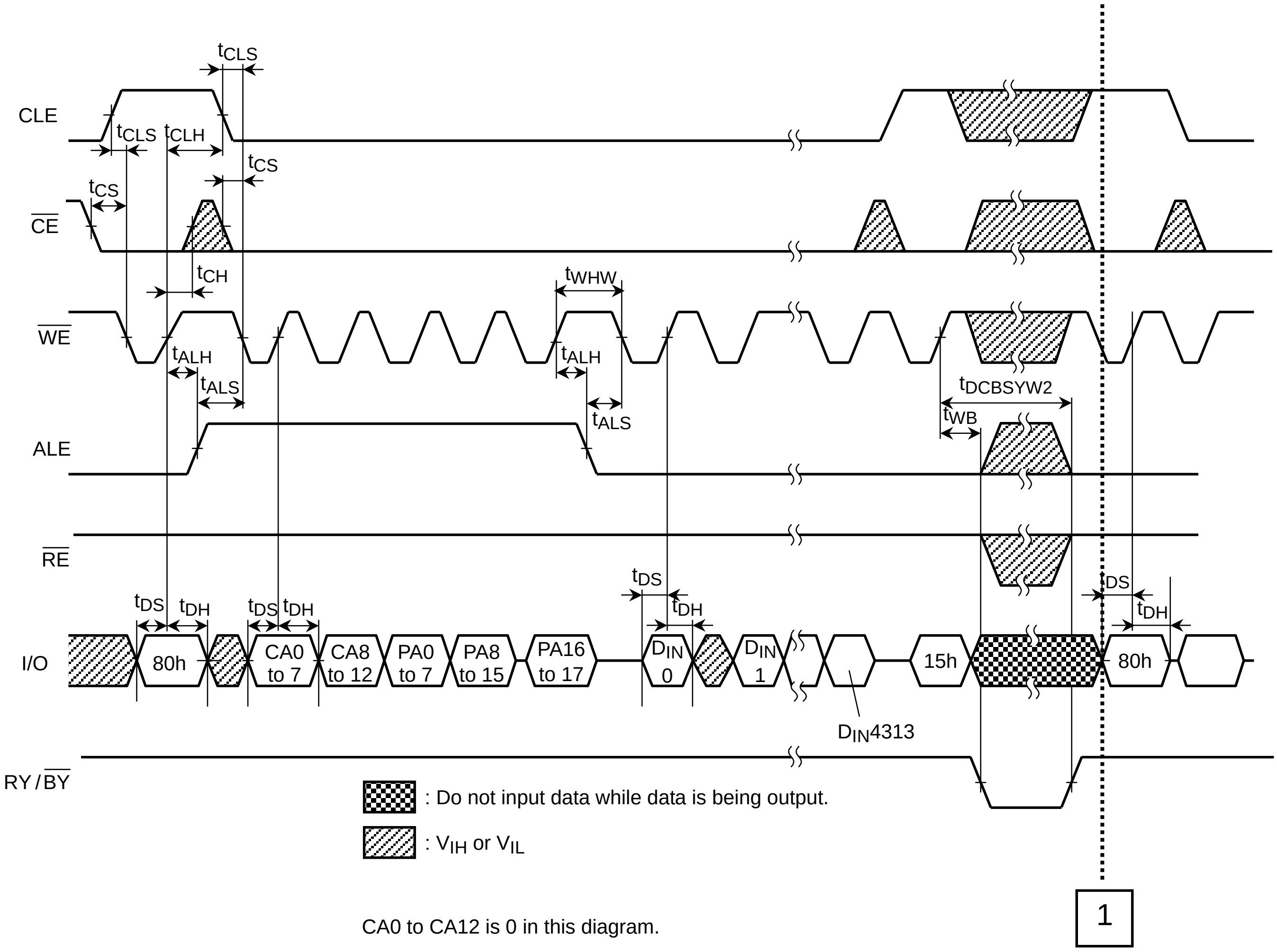


▩ : Do not input data while data is being output.

▨ : V_{IH} or V_{IL}

*) M: up to 4313 (byte input data for ×8 device).

Auto-Program Operation with Data Cache Timing Diagram (1/3)



CA0 to CA12 is 0 in this diagram.

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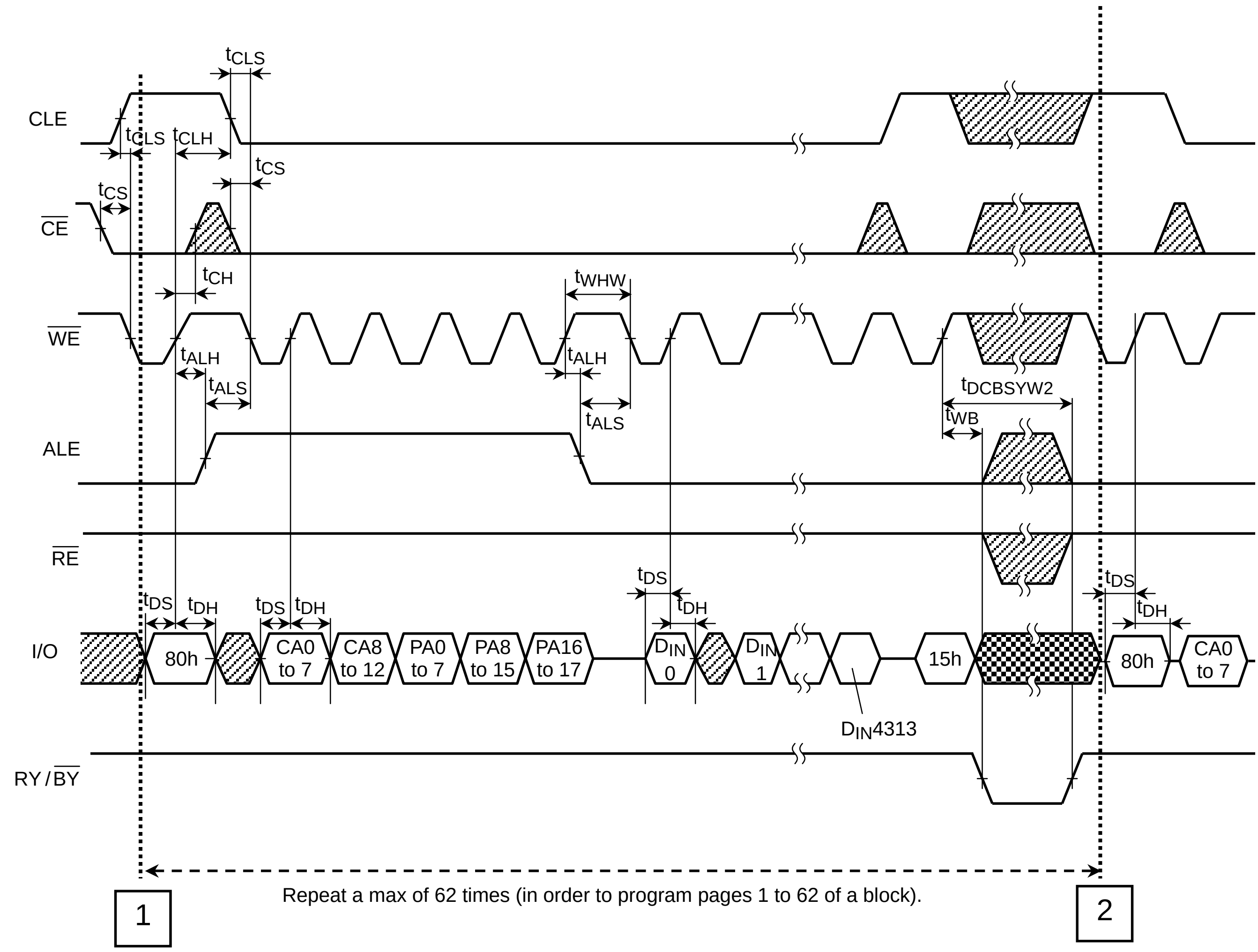
Auto-Program Operation with Data Cache Timing Diagram (2/3)



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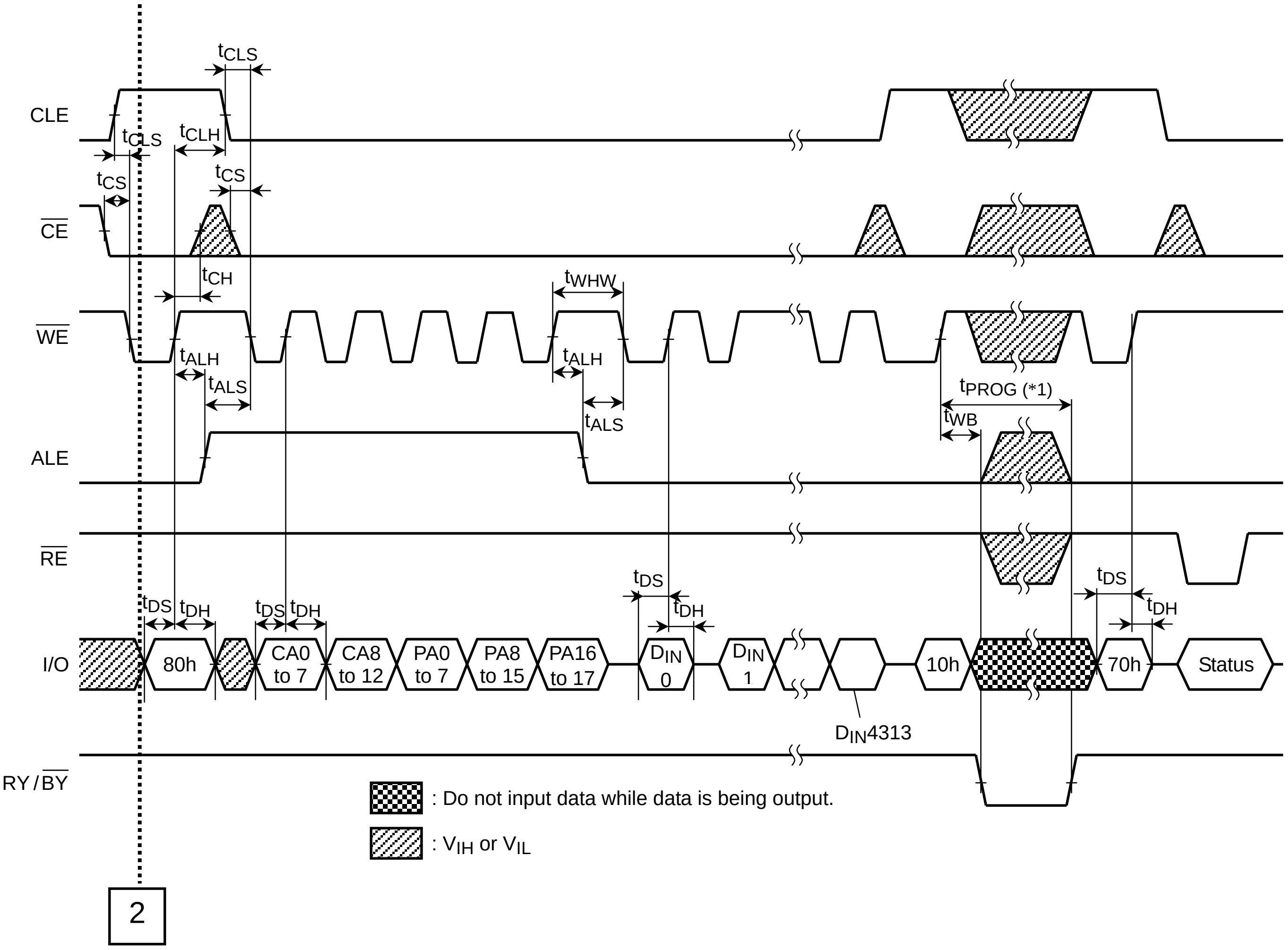
▩ : Do not input data while data is being output.

▨ : V_{IH} or V_{IL}

Auto-Program Operation with Data Cache Timing Diagram (3/3)



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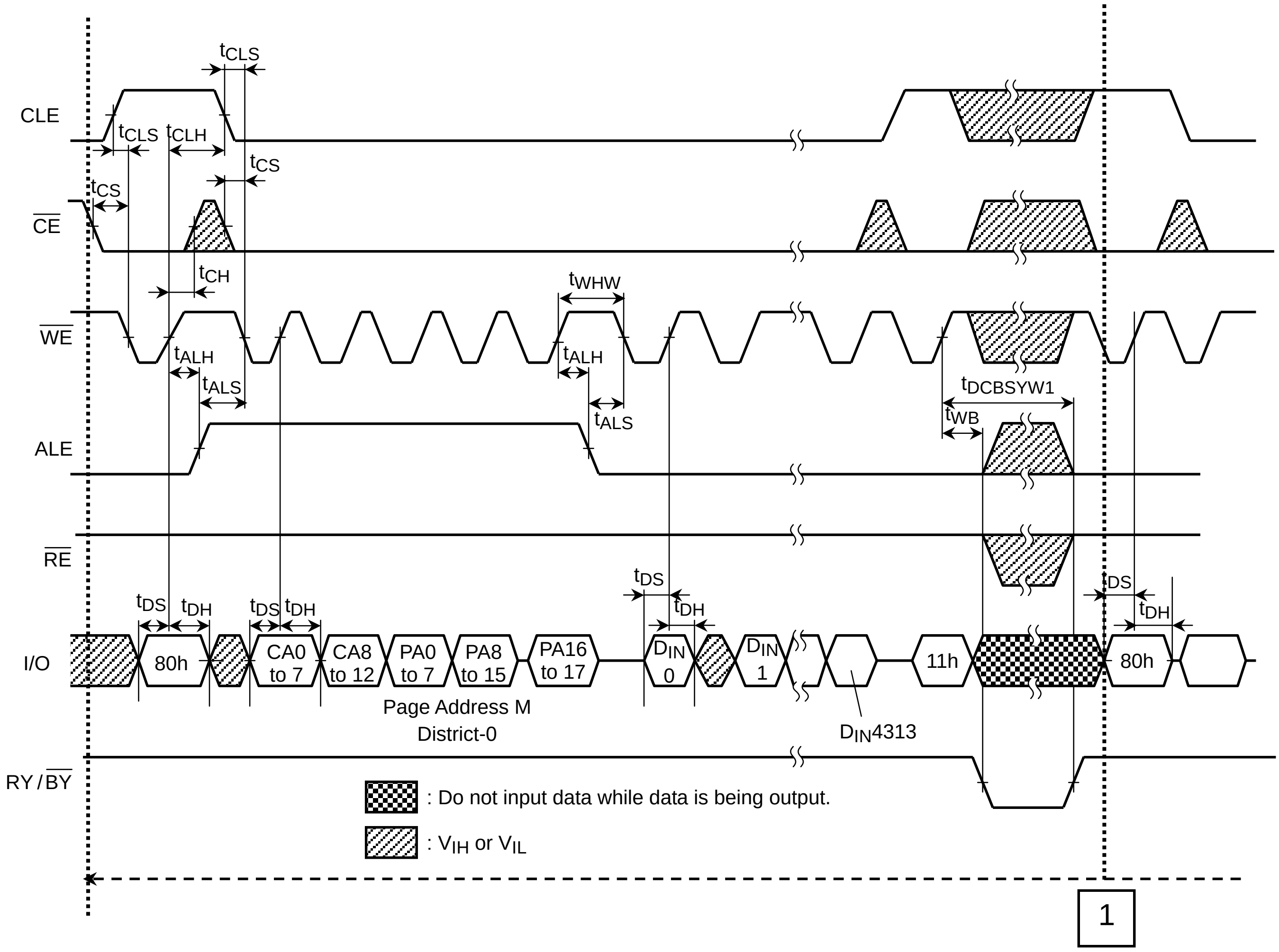
(*1) t_{PROG}: Since the last page programming by 10h command is initiated after the previous cache program, the t_{PROG} during cache programming is given by the following equation.

t_{PROG} = t_{PROG} of the last page + t_{PROG} of the previous page − A
A = (command input cycle + address input cycle + data input cycle time of the last page)

If "A" exceeds the t_{PROG} of previous page, t_{PROG} of the last page is t_{PROG} max.

Multi-Page Program Operation with Data Cache Timing Diagram (1/4)



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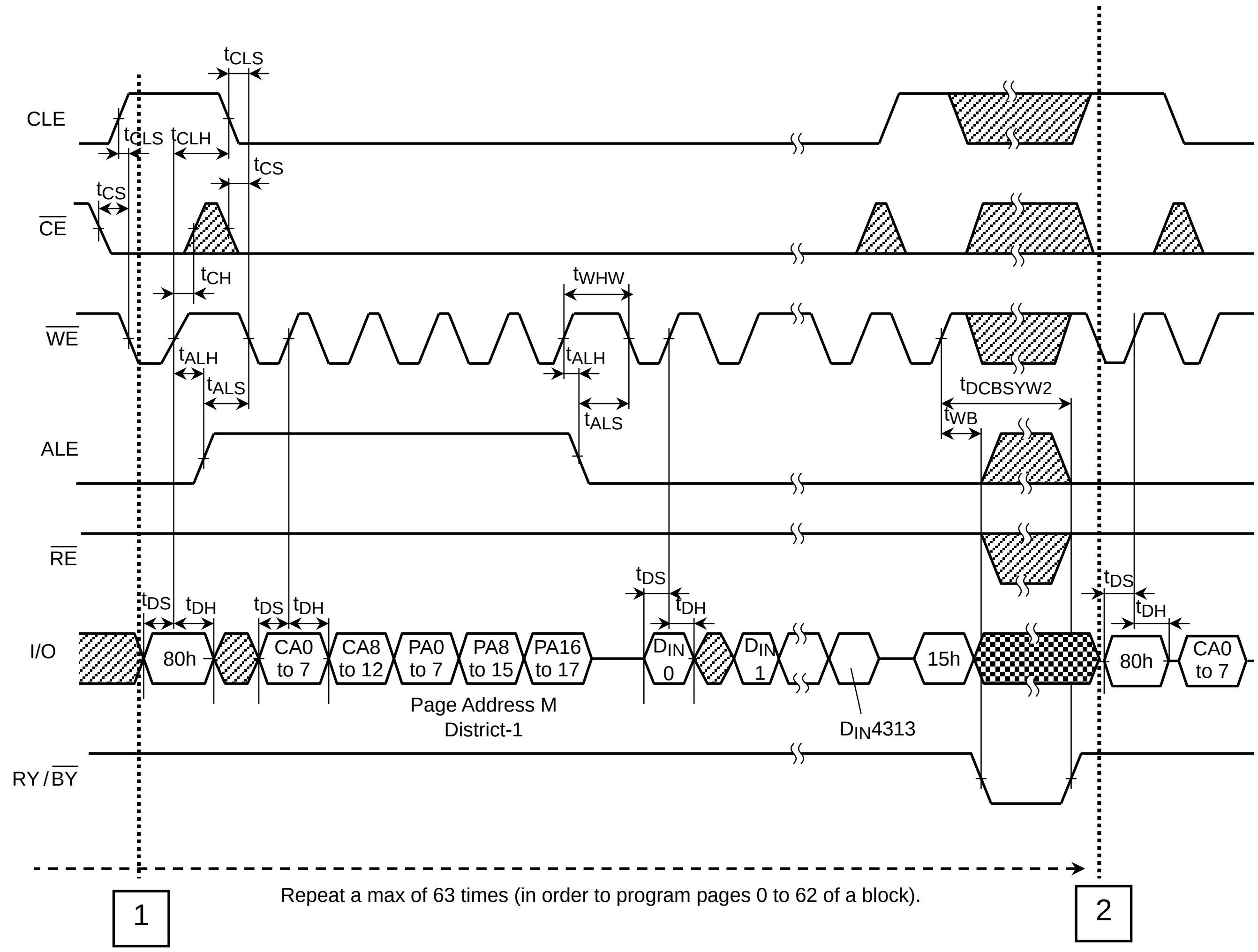
Multi-Page Program Operation with Data Cache Timing Diagram (2/4)



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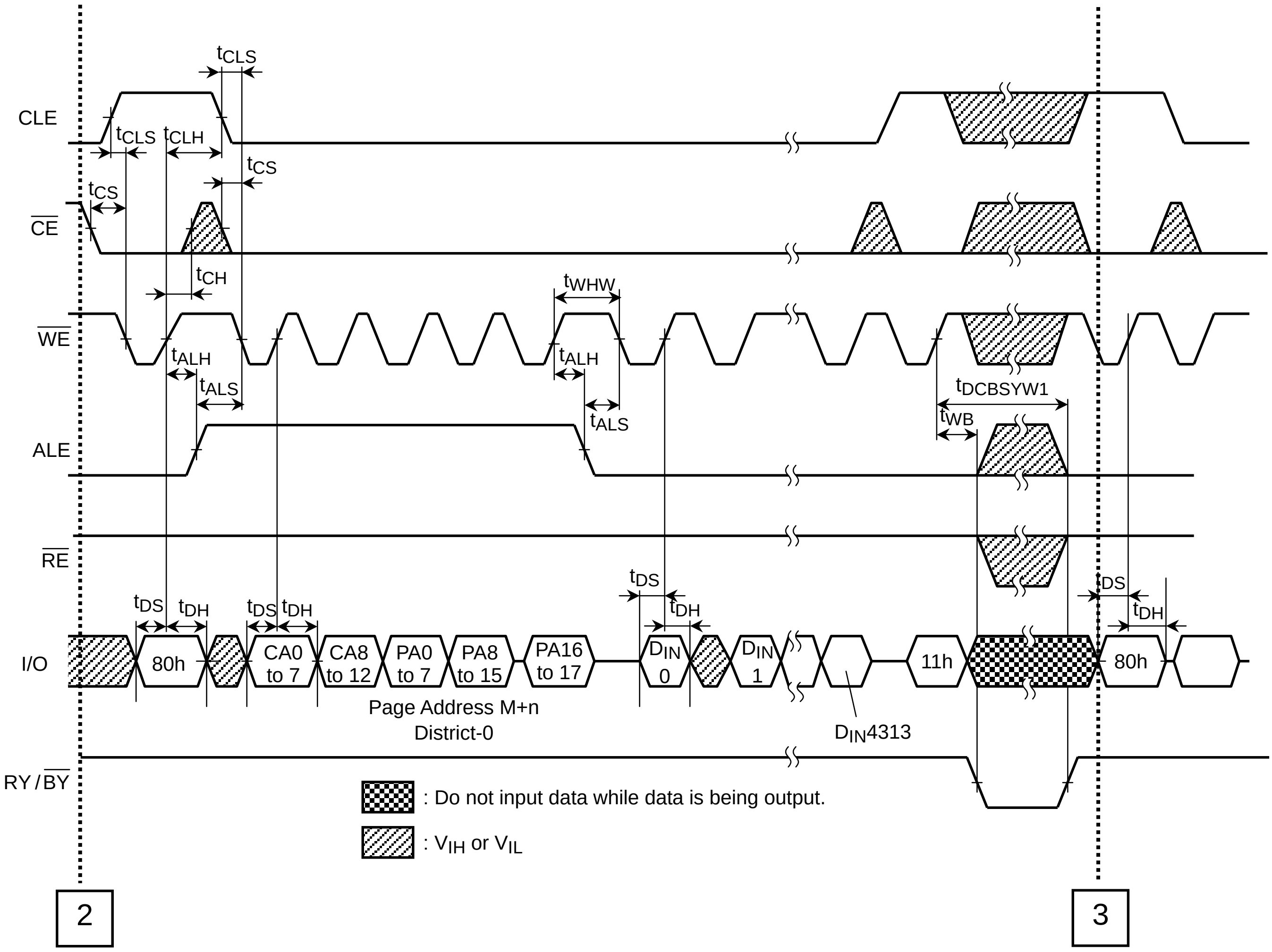
▩ : Do not input data while data is being output.

▨ : V_{IH} or V_{IL}

Multi-Page Program Operation with Data Cache Timing Diagram (3/4)



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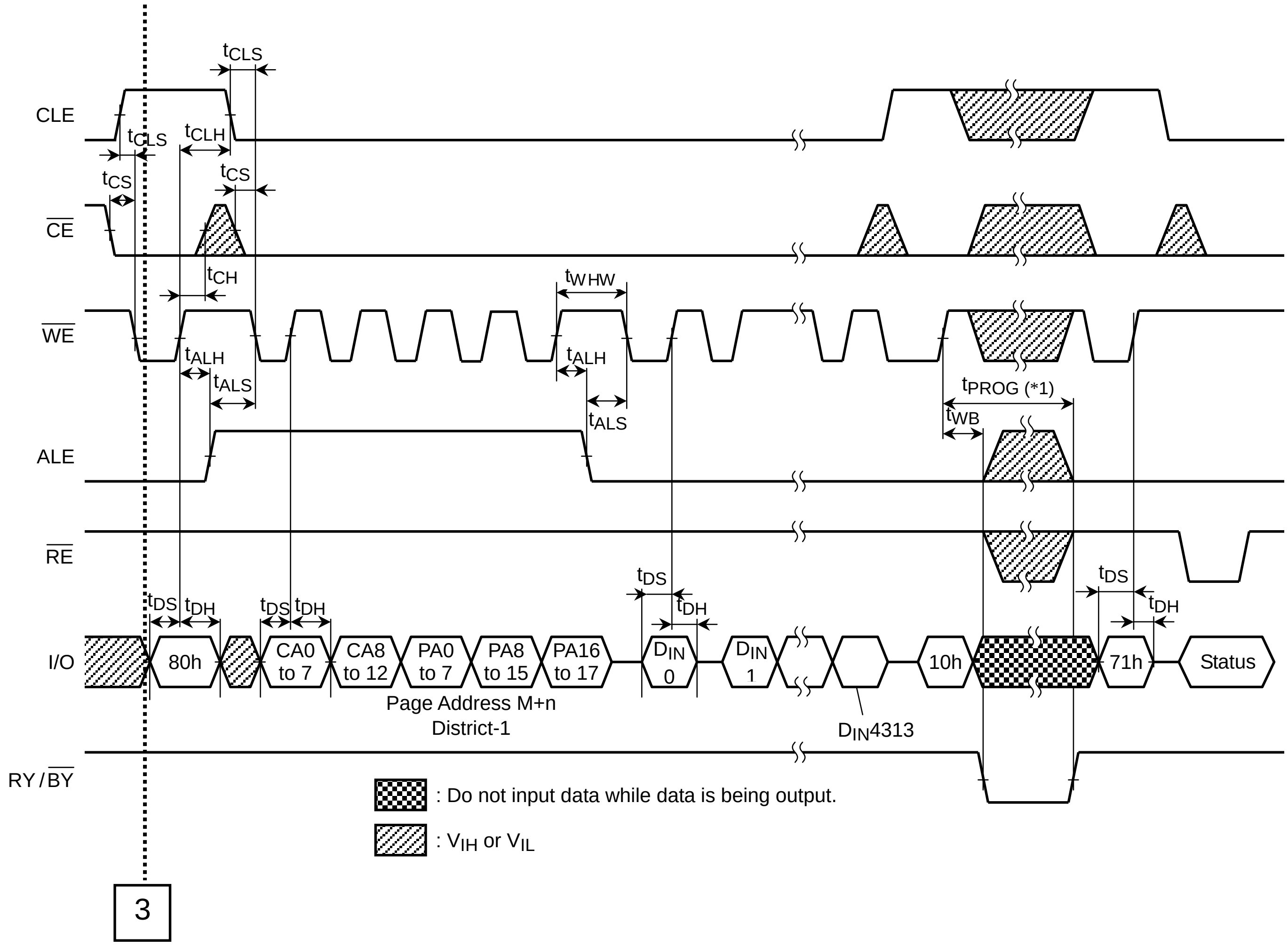
Multi-Page Program Operation with Data Cache Timing Diagram (4/4)



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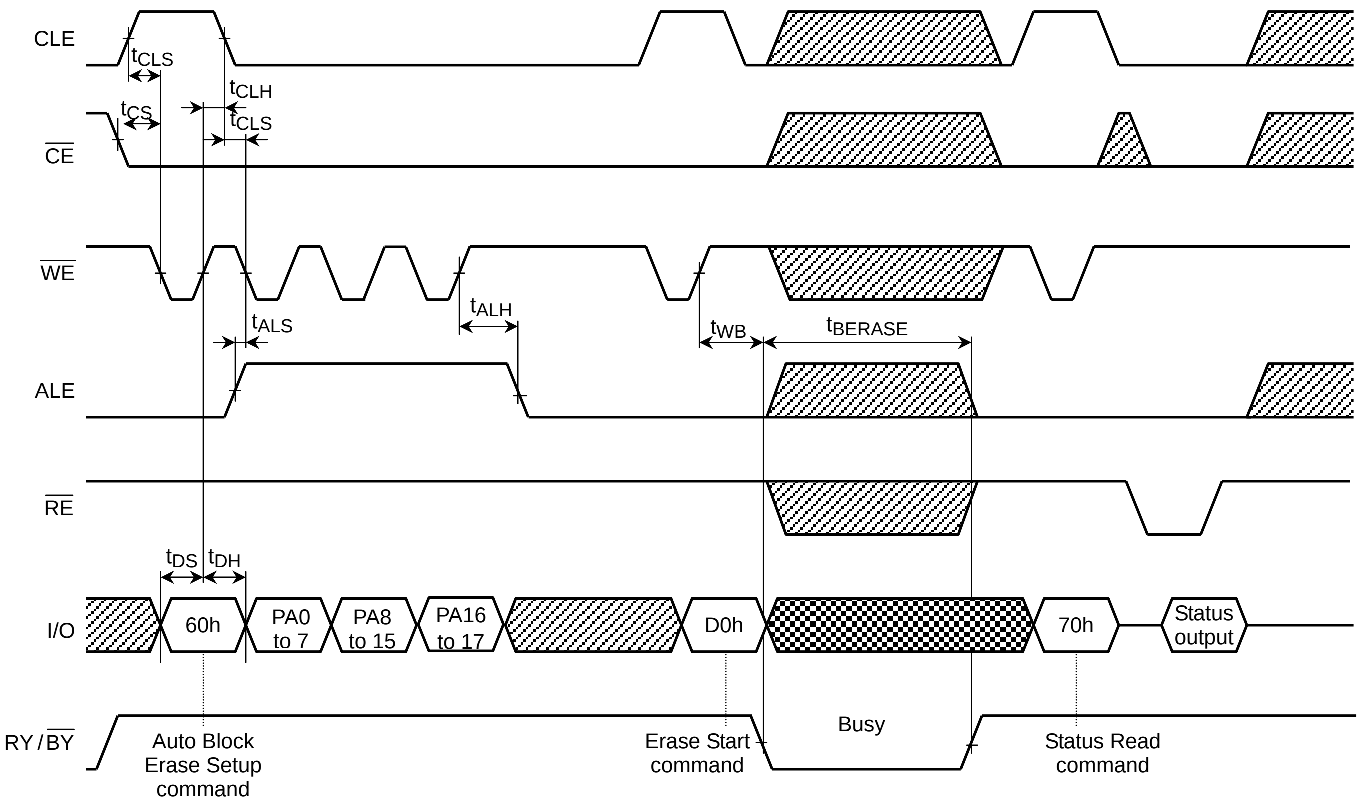
(*1) t_{PROG}: Since the last page programming by 10h command is initiated after the previous cache program, the t_{PROG} during cache
programming is given by the following equation.

$t_{PROG} = t_{PROG}$ of the last page $+$ t_{PROG} of the previous page $-$ A
A $=$ (command input cycle $+$ address input cycle $+$ data input cycle time of the last page)

If “A” exceeds the t_{PROG} of previous page, t_{PROG} of the last page is t_{PROG} max.

(Note) Make sure to terminate the operation with 80h-10h command sequence.
If the operation is terminated by 80h-15h command sequence, monitor I/O 6 (Ready / Busy) by issuing Status Read command (70h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.

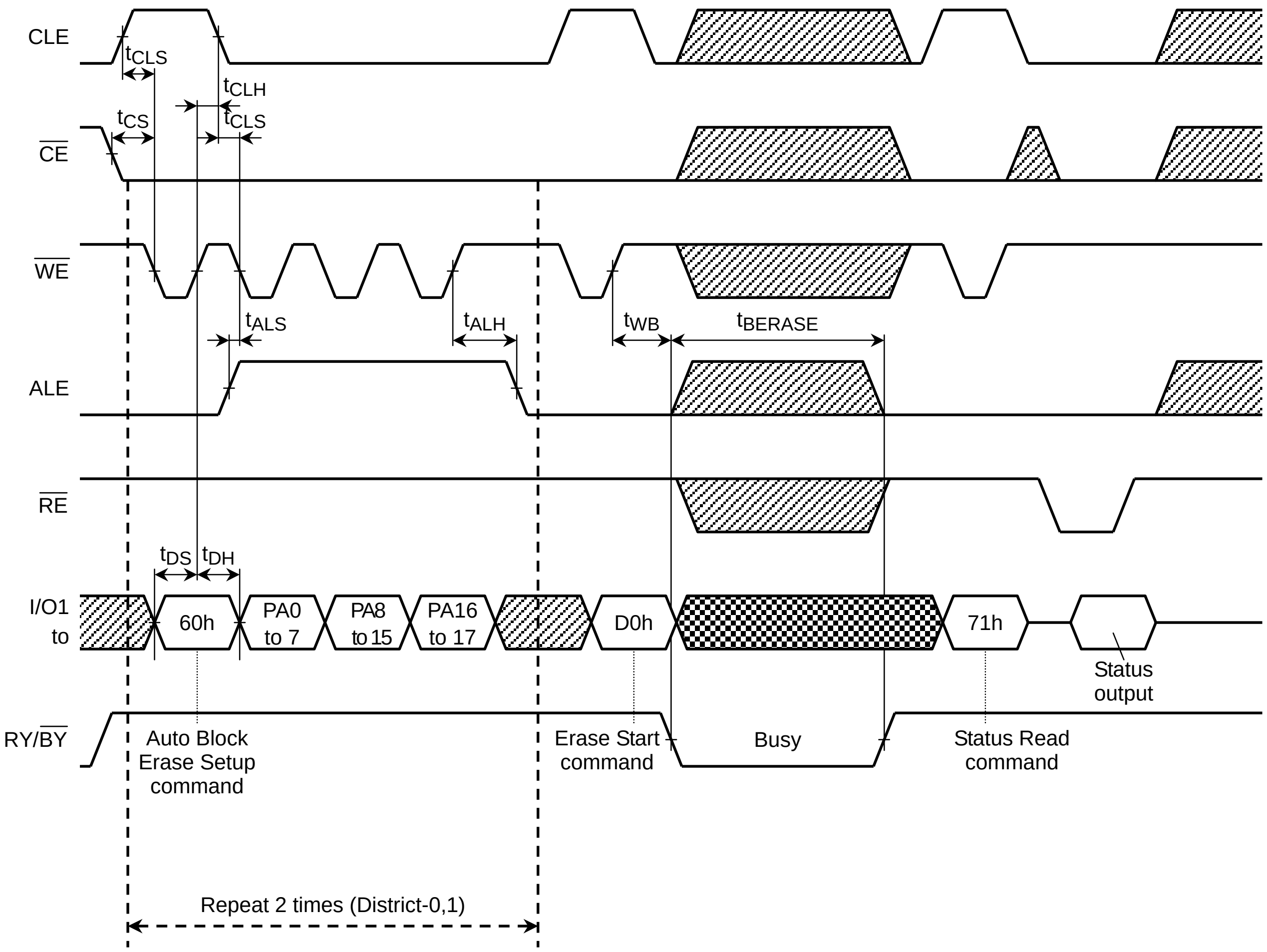
Auto Block Erase Timing Diagram



▨ : V_{IH} or V_{IL}

▦ : Do not input data while data is being output.

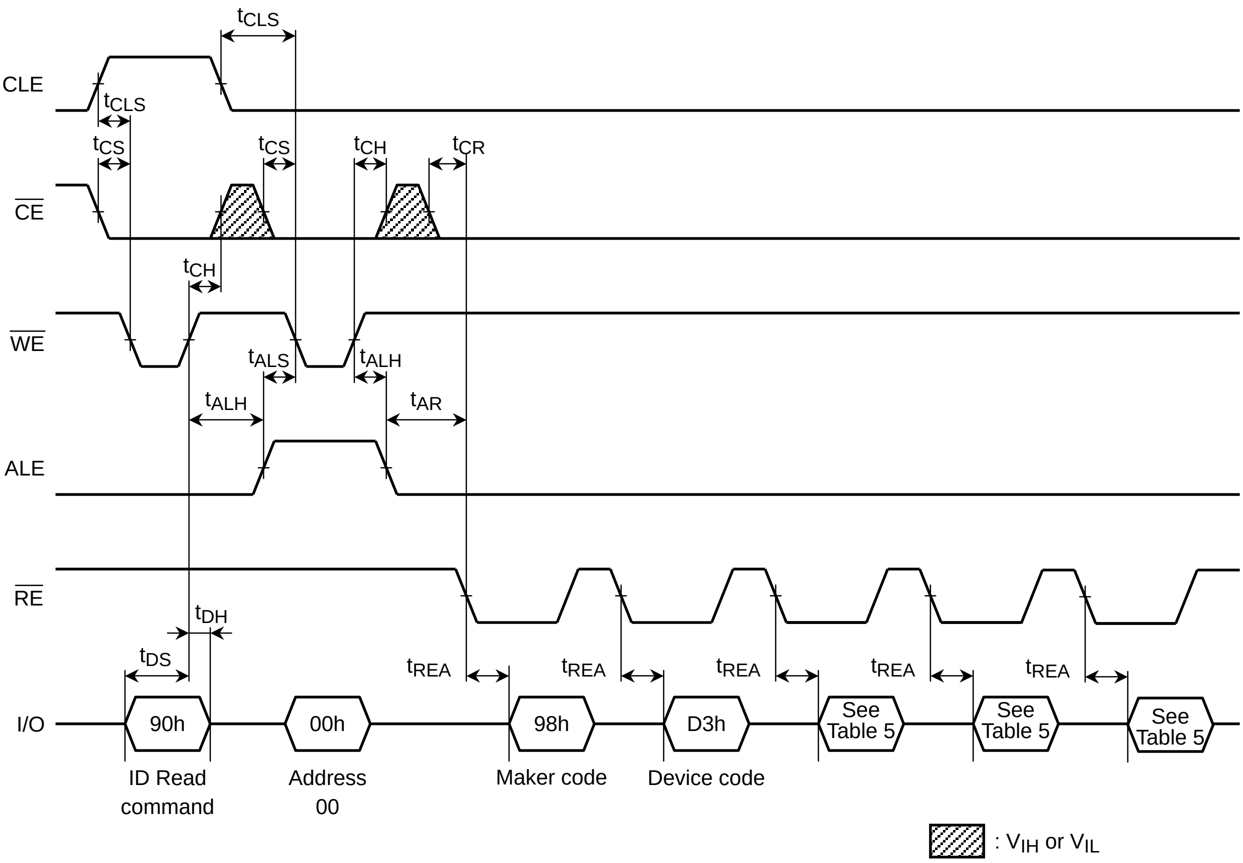
Multi Block Erase Timing Diagram



▨ : V_{IH} or V_{IL}

▩ : Do not input data while data is being output.

ID Read Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge of $\overline{WE}$ while ALE is High.

Chip Enable: $\overline{CE}$ (n)

Since the device contains two 8Gbit chips, control for each chip by using $\overline{CE}$ 1 and $\overline{CE}$ 2. The chip not to be selected is disabled while $\overline{CE}$ is High.
$\overline{CE}$ (n) signal is used to select the chip, and the chip goes into a low-power Standby mode when $\overline{CE}$ goes High during the chip is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state (RY / $\overline{BY}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address = Address + l) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: RY / $\overline{BY}$ (n)

The RY / $\overline{BY}$ output signal is used to indicate the operating condition of the device. The RY / $\overline{BY}$ signal is in Busy state (RY / $\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state (RY / $\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to Vccq with an appropriate resister.
The device has RY / $\overline{BY}$ 1 and RY / $\overline{BY}$ 2 signal. RY / $\overline{BY}$ 1 indicates operating condition of the chip which has $\overline{CE}$ 1, and RY / $\overline{BY}$ 2 indicates operating condition of the chip which has $\overline{CE}$ 2.

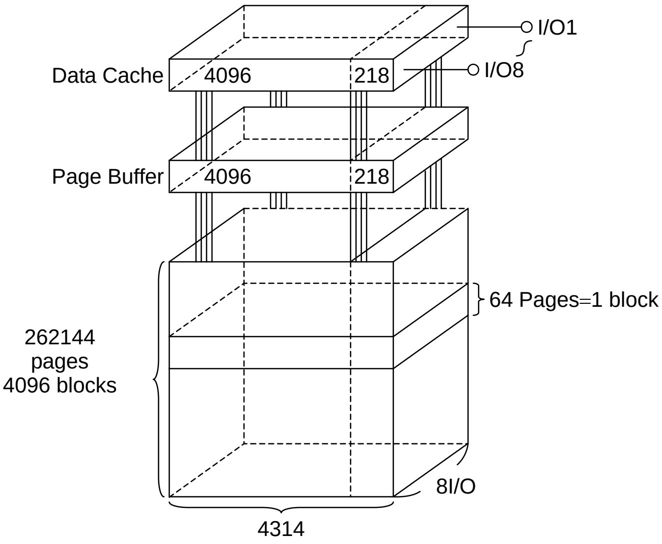
Power on Select: PSL

The PSL signal is used to select whether the device initialization should take place during the device power on or during the first Reset. Please refer to the application note (2) for details.

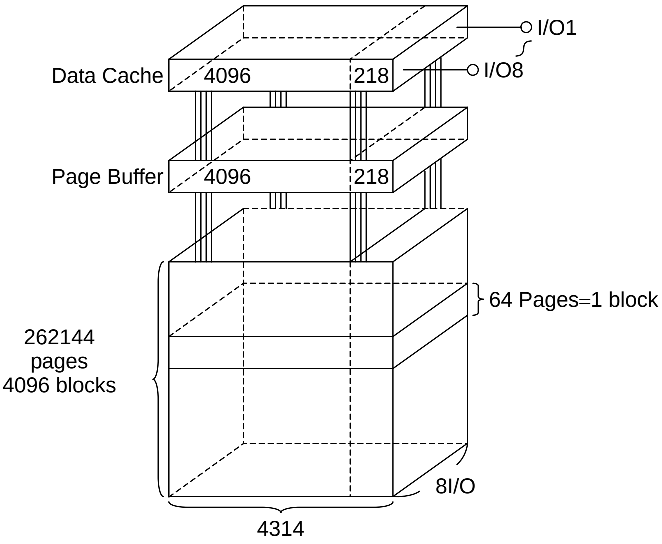
Schematic Cell Layout and Address Assignment

Structure of the device is as follows. The Program operation works on page units while the Erase operation works on block units at each chip.

[8Gbit (Chip A)]



[8Gbit (Chip B)]



A page consists of 4314 bytes in which 4096 bytes are used for main memory storage and 218 bytes are for redundancy or for other uses.

1 page = 4314 bytes
1 block = 4314 bytes × 64 pages = (256K + 13.6K) bytes
Capacity = 4314 bytes × 64pages × 8192 blocks

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	L	CA12	CA11	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8
Fifth cycle	L	L	L	L	L	L	PA17	PA16

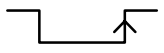
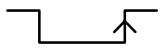
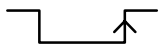
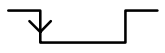
CA0 to CA12: Column address
PA0 to PA17: Page address

PA6 to PA17: Block address
PA0 to PA5: NAND address in block

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ [*1]	PSL [*3]
Command Input	H	L	L		H	*	0V/ V_{CC}/ NU
Data Input	L	L	L		H	H	0V/ V_{CC}/ NU
Address input	L	H	L		H	*	0V/ V_{CC}/ NU
Serial Data Output	L	L	L	H		*	0V/ V_{CC}/ NU
During Program (Busy)	*	*	*	*	*	H	0V/ V_{CC}/ NU
During Erase (Busy)	*	*	*	*	*	H	0V/ V_{CC}/ NU
During Read (Busy)	*	*	H	*	*	*	0V/ V_{CC}/ NU
	*	*	L	H (*2)	H (*2)	*	0V/ V_{CC}/ NU
Program, Erase Inhibit	*	*	*	*	*	L	0V/ V_{CC}/ NU
Standby	*	*	H	*	*	0 V/V_{CC}	0V/ V_{CC}/ NU

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit

*2: If $\overline{CE}$ is low during read busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read command can be input during Read Busy.

*3: PSL must be tied to either 0V or Vcc, or left unconnected (NU).

Table 3. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read	00	30	
Column Address Change in Serial Data Output	05	E0	
Read with Data Cache	31	—	
Read Start for Last Page in Read Cycle with Data Cache	3F	—	
Auto Page Program	80	10	
Column Address Change in Serial Data Input	85	—	
Auto Program with Data Cache	80	15	
Multi Page Program	80	11	
Read for Page Copy (2)	00	3A	
Auto Program with Data Cache during Page Copy (2)	8C	15	
Auto Program for last page during Page Copy (2)	8C	10	
Auto Block Erase	60	D0	
ID Read	90	—	
Status Read	70	—	○
Status Read for Multi-Page Program or Multi Block Erase	71	—	○
Reset	FF	—	○

HEX data bit assignment

(Example)

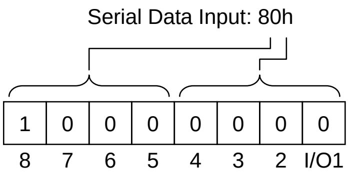


Table 4 shows the operation states for Read mode, when tREH is long.

Table 4. Read mode operation states

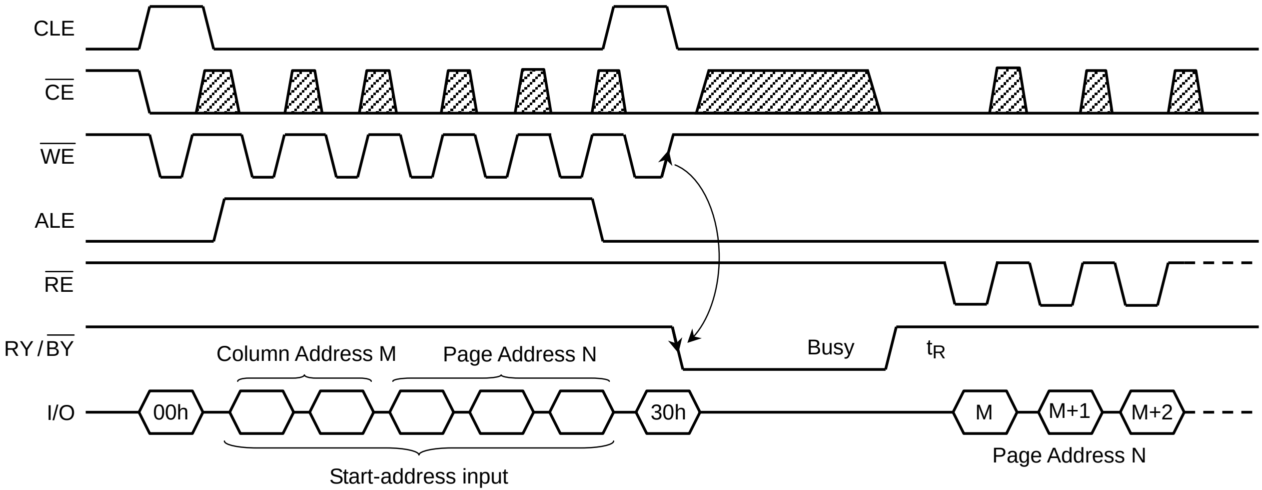
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O8	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

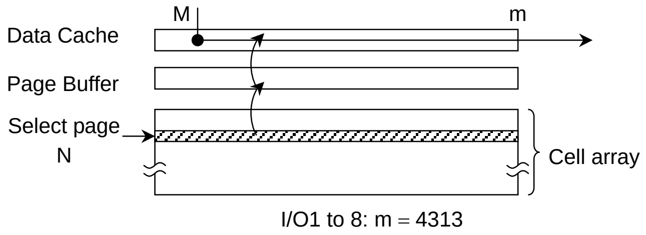
H: V_{IH}, L: V_{IL}

DEVICE OPERATION

Read Mode

Read mode is set when the "00h" and “30h” commands are issued to the Command register. Between the two commands, a start address for the Read mode needs to be issued. Refer to the figures below for the sequence and the block diagram (Refer to the detailed timing chart.).

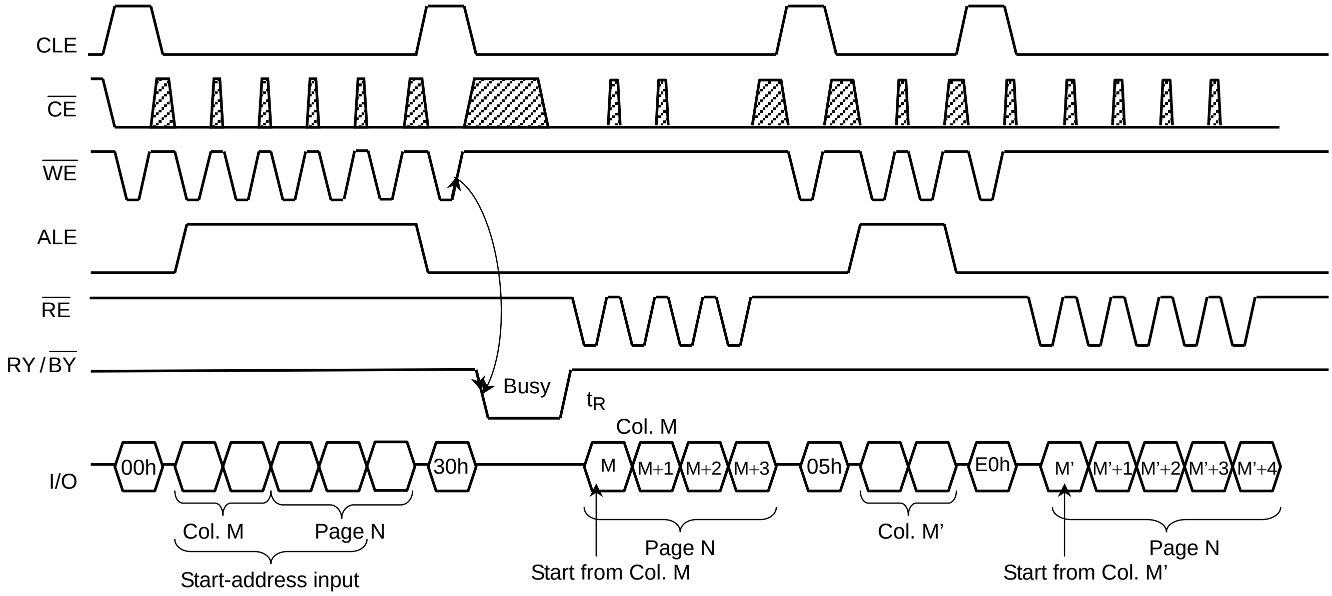


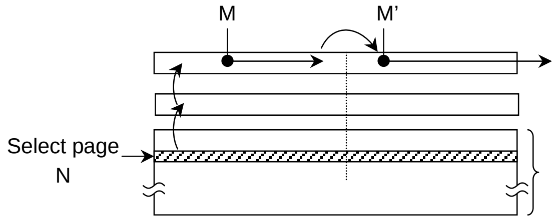


A data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of WE in the 30h command input cycle (after the address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the RE clock from the start address designated in the address input cycle.

Random Column Address Change in Read Cycle

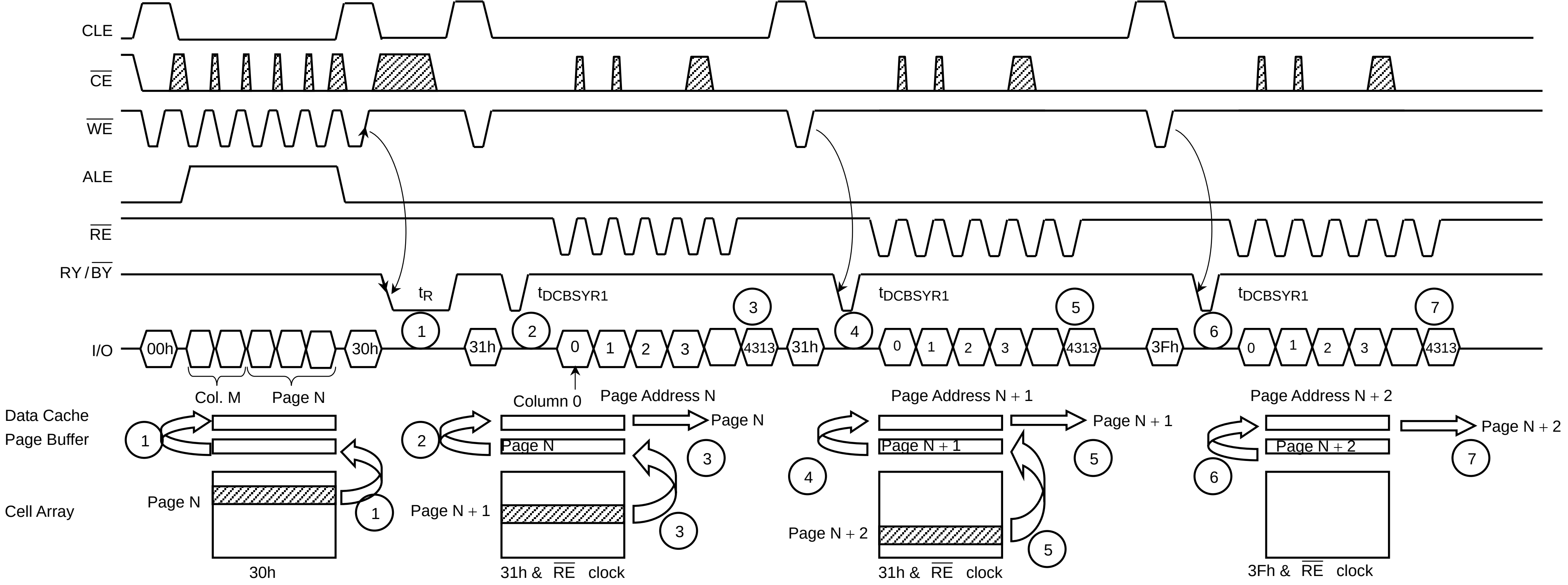




During the serial data output from the Data Cache, the column address can be changed by inputting a new column address using the 05h and E0h commands. The data is read out in serial starting at the new column address. Random Column Address Change operation can be done multiple times within the same page.

Read Operation with Read Cache

The device has a Read operation with Data Cache that enables the high speed read operation shown below. When the block address changes, this sequence has to be started from the beginning.



If the 31h command is issued to the device, the data content of the next page is transferred to the Page Buffer during serial data out from the Data Cache, and therefore the tR (Data transfer from memory cell to data register) will be reduced.

1 Normal read. Data is transferred from Page N to Data Cache through Page Buffer. During this time period, the device outputs Busy state for tR max.

2 After the Ready/Busy returns to Ready, 31h command is issued and data is transferred to Data Cache from Page Buffer again. This data transfer takes tDCBSYR1 max and the completion of this time period can be detected by Ready/Busy signal.

3 Data of Page N + 1 is transferred to Page Buffer from cell while the data of Page N in Data cache can be read out by /RE clock simultaneously.

4 The 31h command makes data of Page N + 1 transfer to Data Cache from Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max.. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.

5 Data of Page N + 2 is transferred to Page Buffer from cell while the data of Page N + 1 in Data cache can be read out by /RE clock simultaneously

6 The 3Fh command makes the data of Page N + 2 transfer to the Data Cache from the Page Buffer after the completion of the transfer from cell to Page Buffer. The device outputs Busy state for tDCBSYR1 max.. This Busy period depends on the combination of the internal data transfer time from cell to Page buffer and the serial data out time.

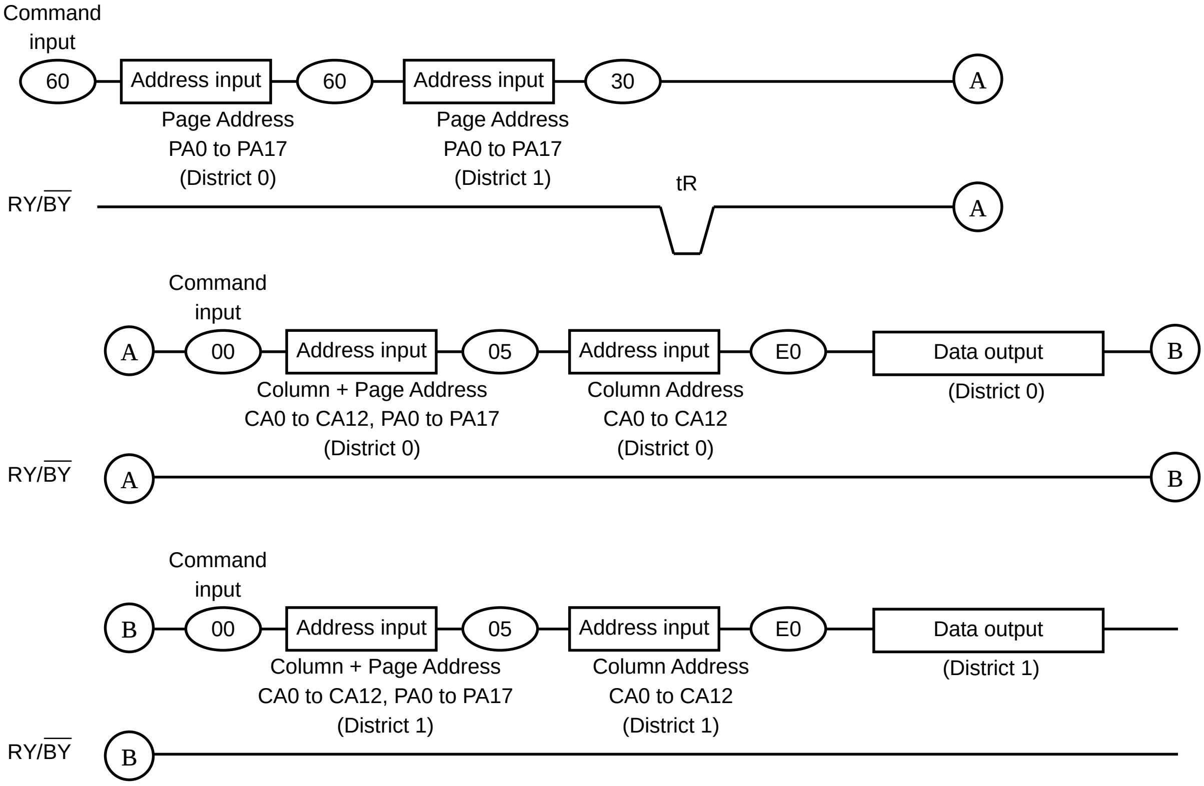
7 Data of Page N + 2 in Data Cache can be read out, but since the 3Fh command does not transfer the data from the memory cell to Page Buffer, the device can accept new command input immediately after the completion of serial data out.

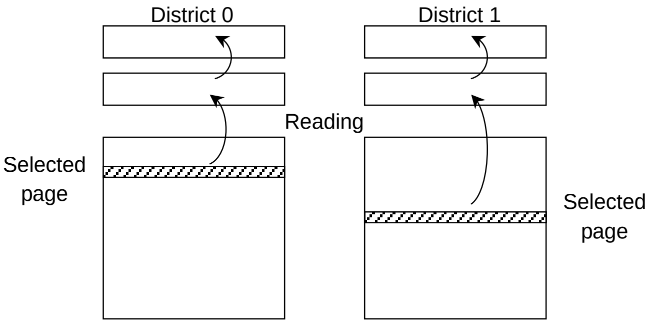
Multi Page Read Operation

The device has a Multi Page Read operation and Multi Page Read with Data Cache operation..
This operation is limited in each internal chip (e.g. within chip A).

(1) Multi Page Read without Data Cache

The sequence of command and address input is shown below.
Same page address (PA0 to PA5) within each district has to be selected.



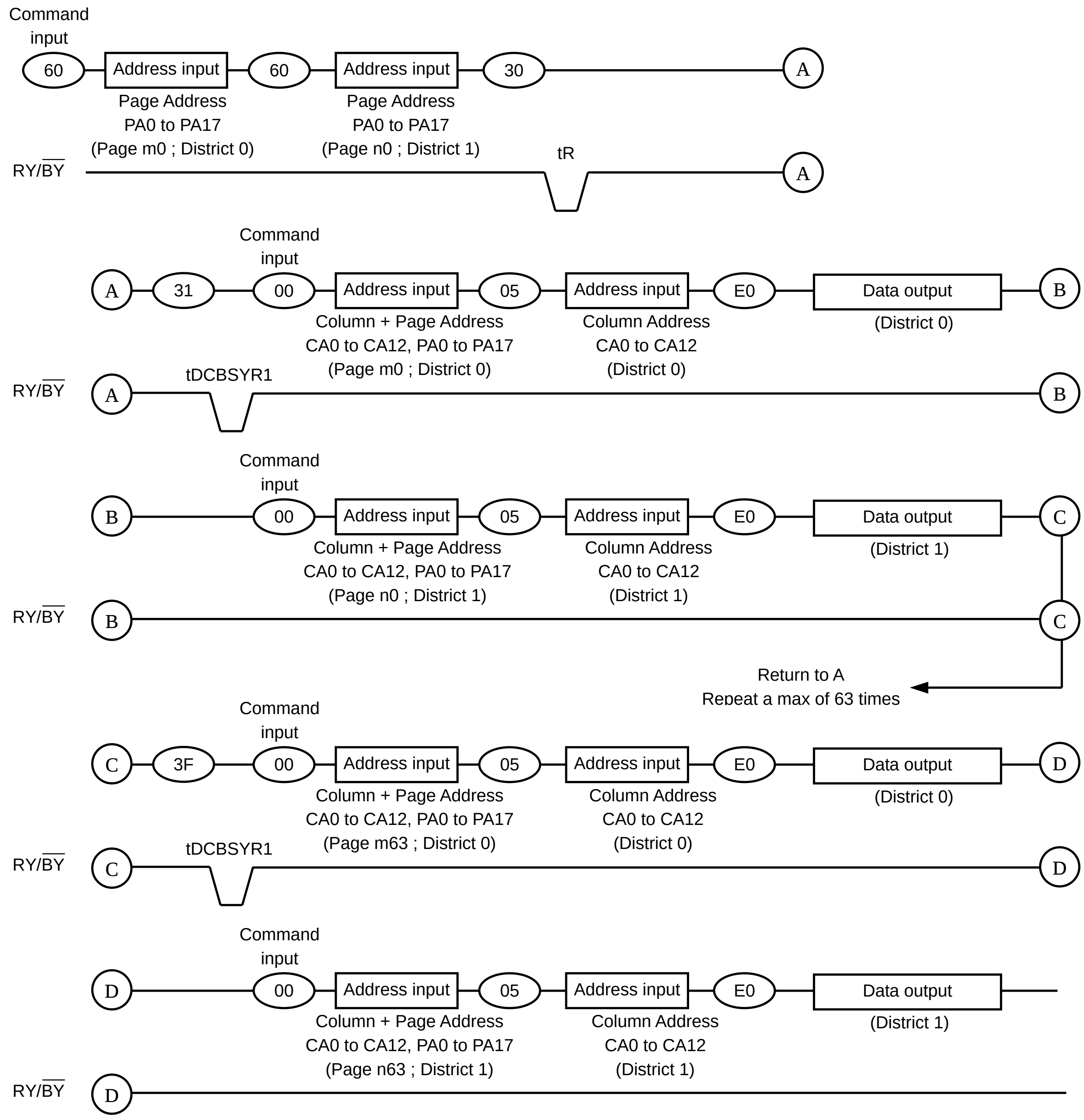


The data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the 2 Districts address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle.

(2) Multi Page Read with Data Cache

When the block address changes (increments) this sequenced has to be started from the beginning.
The sequence of command and address input is shown below.
Same page address (PA0 to PA5) within each district has to be selected.



(3) Notes

(a) Internal addressing in relation with the Districts

To use Multi Page Read operation, the internal addressing should be considered in relation with the District.

- The device contains two chips of NAND EEPROM.
- Each internal chip consists from 2 Districts.
- Each District consists from 2048 erase blocks.
- The allocation rule is follows.
  District 0: Block 0, Block 1, Block 2, Block 3,···, Block 2047
  District 1: Block 2048, Block 2049, Block 2050, Block 2051,···, Block 4095

(b) Address input restriction for the Multi Page Read operation

There are following restrictions in using Multi Page Read;

(Restriction)
Maximum one block should be selected from each District.
Same page address (PA0 to PA5) within two districts has to be selected.
For example;
(60) [District 0, Page Address 0x00000] (60) [District 1, Page Address 0x20000] (30)
(60) [District 0, Page Address 0x00001] (60) [District 1, Page Address 0x20001] (30)

(Acceptance)
There is no order limitation of the District for the address input.
For example, following operation is accepted;
(60) [District 0] (60) [District 1] (30)
(60) [District 1] (60) [District 0] (30)

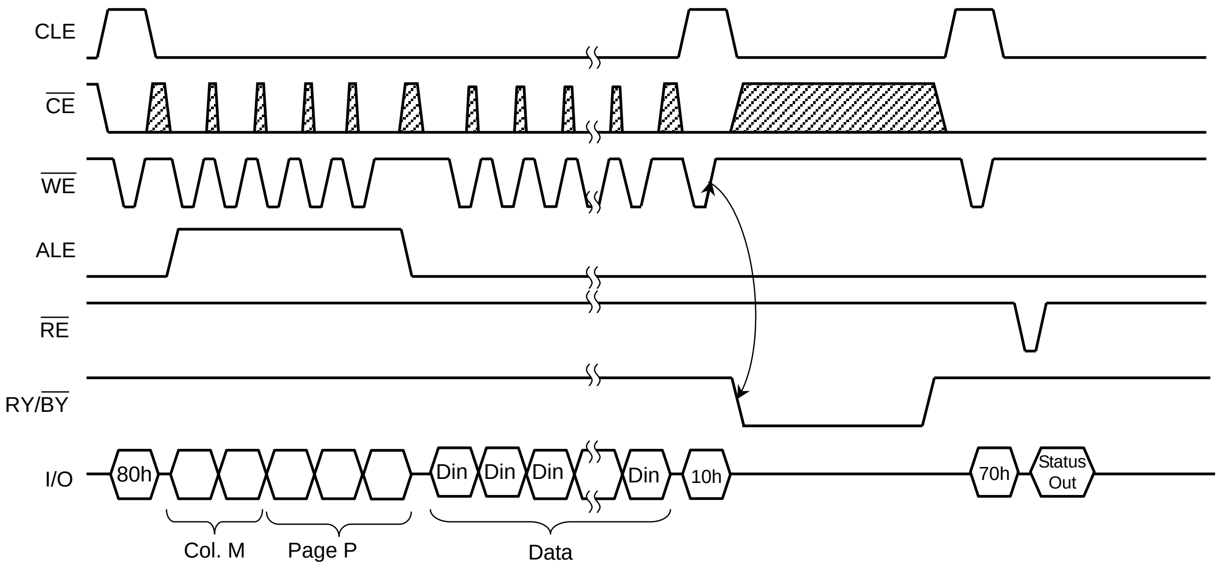
It requires no mutual address relation between the selected blocks from each District.

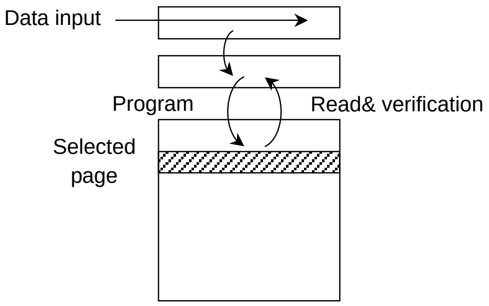
(c) $\overline{\text{WP}}$ signal

Make sure $\overline{\text{WP}}$ is held to High level when Multi Page Read operation is performed

Auto Page Program Operation

The device carries out an Automatic Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)



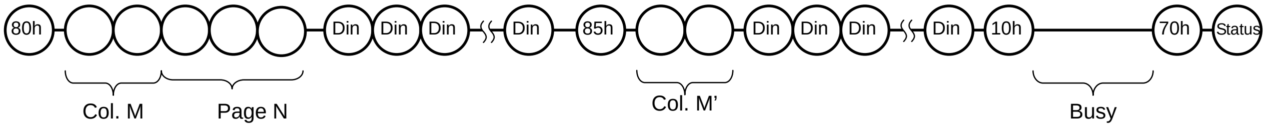


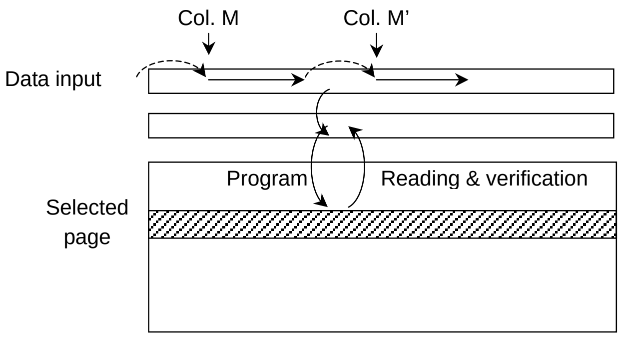
The data is transferred (programmed) from the Data Cache via the Page Buffer to the selected page on the rising edge of WE following input of the “10h” command. After programming, the programmed data is transferred back to the Page Buffer to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Random Column Address Change in Auto Page Program Operation

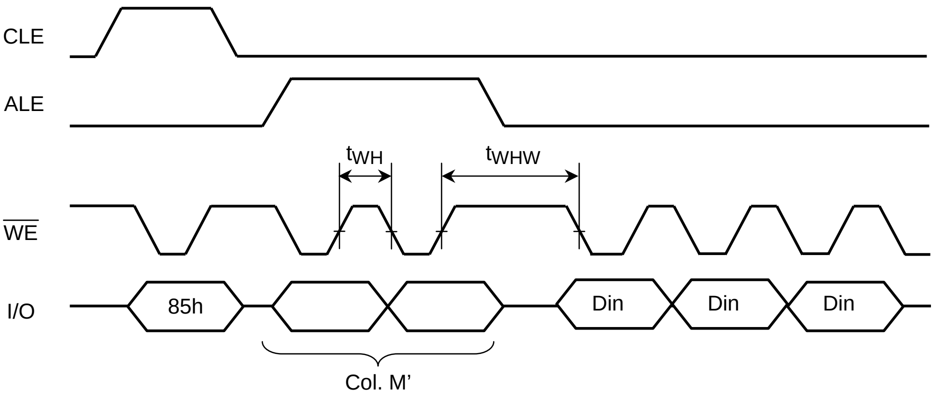
The column address can be changed by the 85h command during the data input sequence of the Auto Page Program operation.

Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.



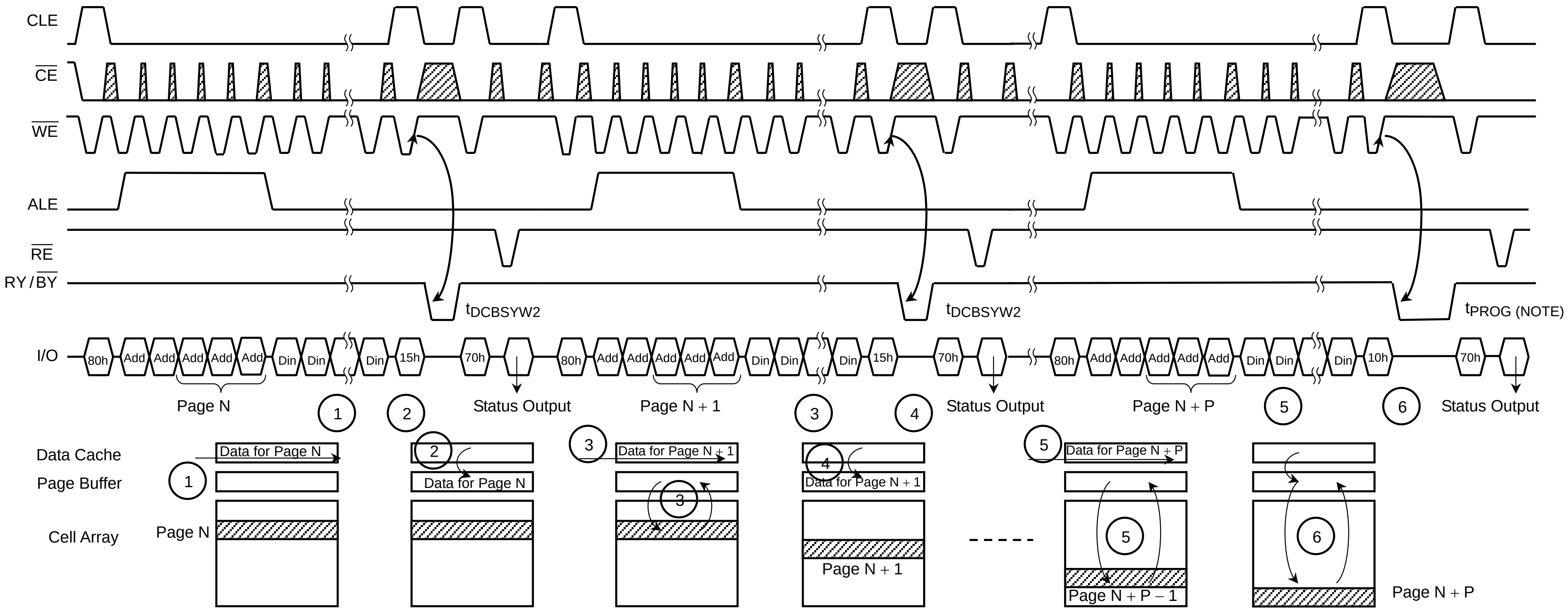


tWHW is the time from the the $\overline{\text{WE}}$ rising edge of final address cycle to the $\overline{\text{WE}}$ falling edge of first data cycle. $\overline{\text{WE}}$ High Hold Time for the final address input after 85h command is also needed more time (tWHW) than tWH.



Auto Page Program Operation with Data Cache

The device has an Auto Page Program with Data Cache operation enabling the high speed program operation shown below. When the block address changes this sequenced has to be started from the beginning.



Issuing the 15h command to the device after serial data input initiates the program operation with Data Cache

1 Data for Page N is input to Data Cache.

2 Data is transferred to the Page Buffer by the 15h command. During the transfer the Ready/Busy outputs Busy State ($t_{DCBSYW2}$).

3 Data is programmed to the selected page while the data for page N + 1 is input to the Data Cache.

4 By the 15h command, the data in the Data Cache is transferred to the Page Buffer after the programming of page N is completed. The device output busy state from the 15h command until the Data Cache becomes empty. The duration of this period depends on timing between the internal programming of page N and serial data input for Page N + 1 ($t_{DCBSYW2}$).

5 Data for Page N + P is input to the Data Cache while the data of the Page N + P − 1 is being programmed.

6 The programming with Data Cache is terminated by the 10h command. When the device becomes Ready, it shows that the internal programming of the Page N + P is completed.

NOTE: Since the last page programming by the 10h command is initiated after the previous cache program, the tPROG during cache programming is given by the following;

$t_{PROG} = t_{PROG}$ for the last page + t_{PROG} of the previous page − (command input cycle + address input cycle + data input cycle time of the previous page)

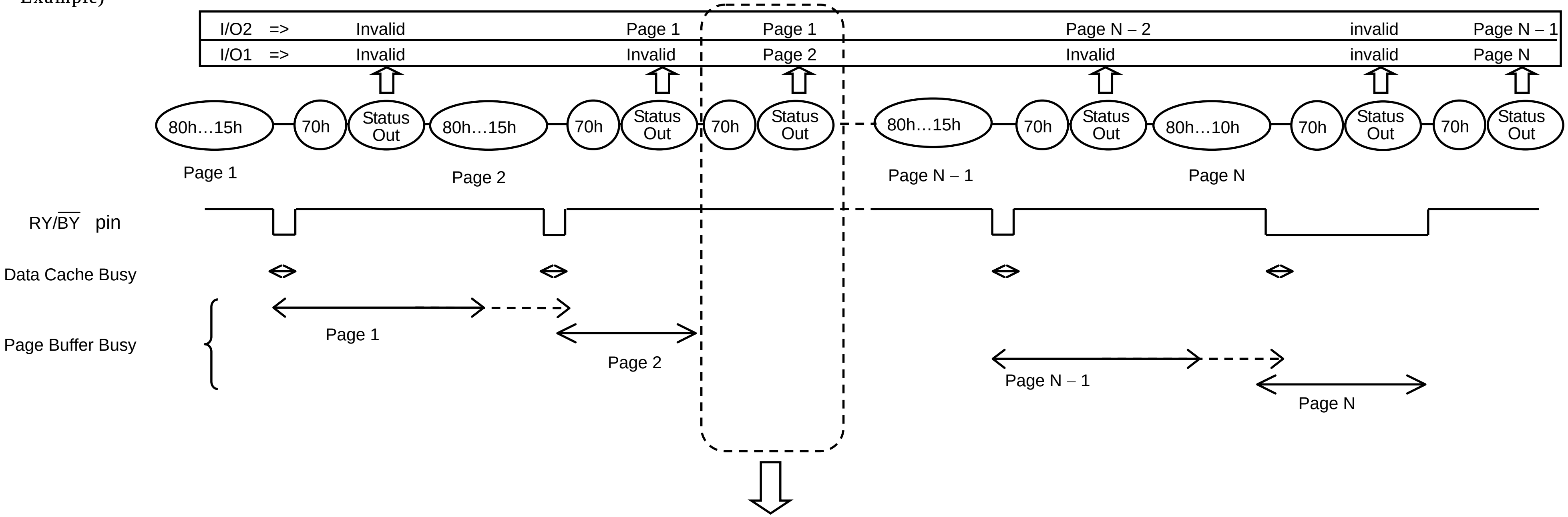
Pass/fail status for each page programmed by the Auto Page Programming with Data Cache operation can be detected by the Status Read operation.

- I/O1 : Pass/fail of the current page program operation.
- I/O2 : Pass/fail of the previous page program operation.

The Pass/Fail status on I/O1 and I/O2 are valid under the following conditions.

- Status on I/O1: Page Buffer Ready/Busy is Ready State.
  The Page Buffer Ready/Busy is output on I/O6 by Status Read operation or $RY/\overline{BY}$ pin after the 10h command
- Status on I/O2: Data Cache Read/Busy is Ready State.
  The Data Cache Ready/Busy is output on I/O7 by Status Read operation or $RY/\overline{BY}$ pin after the 15h command.

Example)

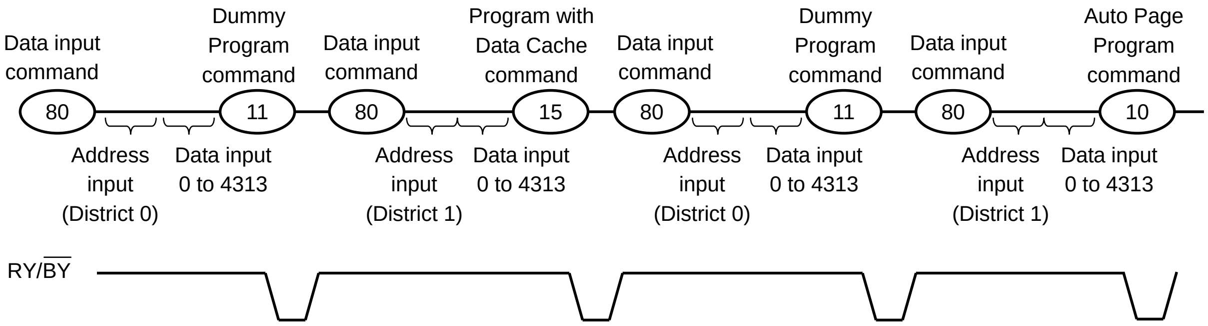


If the Page Buffer Busy returns to Ready before the next 80h command input, and if Status Read is done during this Ready period, the Status Read provides pass/fail for Page 2 on I/O1 and pass/fail result for Page1 on I/O2

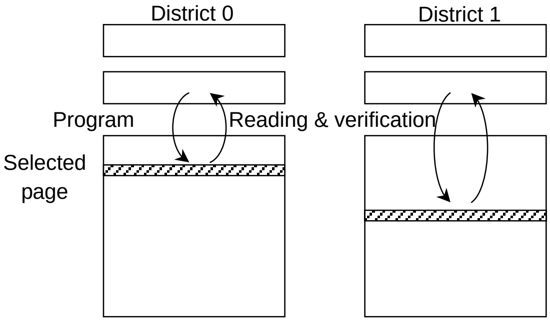
Multi Page Program with Data Cache

The device has a Multi Page Program with Data Cache operation, which enables even higher speed program operation compared to Auto Page Program with Data Cache as shown below. When the block address changes (increments) this sequenced has to be started from the beginning. And this operation is limited in each internal chip (e.g. within chip A).

The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)



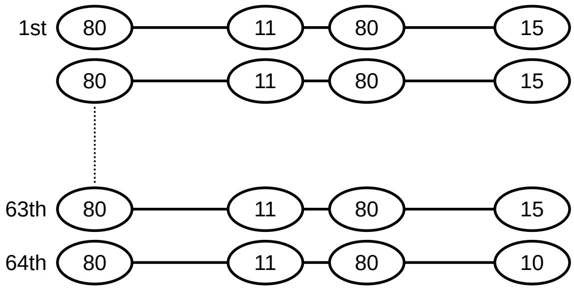
After “15h” or “10h” Program command is input to device, physical programing starts as follows. For details of Auto Program with Data Cache, refer to “Auto Page Program with Data Cache”.



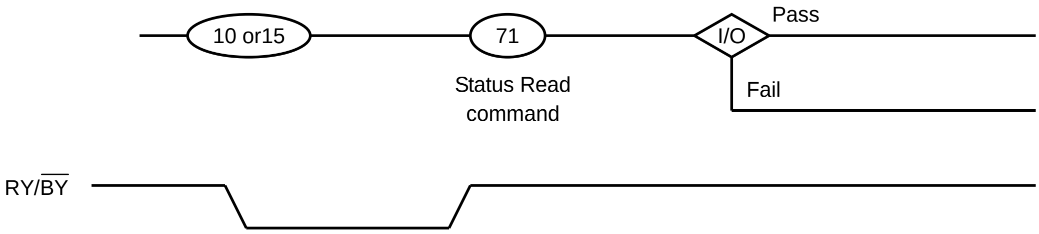
The data is transferred (programmed) from the page buffer to the selected page on the rising edge of -WE following input of the “15h” or “10h” command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Starting the above operation from 1st page of the selected erase blocks, and then repeating the operation total 64 times with incrementing the page address in the blocks, and then input the last page data of the blocks, "10h" command executes final programming. Make sure to terminated with 80h-10h command sequence.

In this full sequence, the command sequence is following.



After the "15h" or "10h" command, the results of the above operation is shown through the "71h"Status Read command.



The 71h command Status description is as below.

	STATUS	OUTPUT	
I/O1	Chip Status1 : Pass/Fail	Pass: 0	Fail: 1
I/O2	District 0 Chip Status1 : Pass/Fail	Pass: 0	Fail: 1
I/O3	District 1 Chip Status1 : Pass/Fail	Pass: 0	Fail: 1
I/O4	District 0 Chip Status2 : Pass/Fail	Pass: 0	Fail: 1
I/O5	District 1 Chip Status2 : Pass/Fail	Pass: 0	Fail: 1
I/O6	Ready/Busy	Ready: 1	Busy: 0
I/O7	Data Cache Ready/Busy	Ready: 1	Busy: 0
I/O8	Write Protect	Protect: 0	Not Protect: 1

I/O1 describes Pass/Fail condition of district 0 and 1(OR data of I/O2 and I/O3). If one of the districts fails during multi page program operation, it shows "Fail".

I/O2 to 5 shows the Pass/Fail condition of each district. For details on "Chip Status1" and "Chip Status2", refer to section "Status Read".

Internal addressing in relation with the Districts

To use Multi Page Program operation, the internal addressing should be considered in relation with the District.

- The device contains two chips of NAND EEPROM.
- Each internal chip consists from 2 Districts.
- Each District consists from 2048 erase blocks.
- The allocation rule is follows.
    District 0: Block 0, Block 1, Block 2, Block 3,···, Block 2047
    District 1: Block 2048, Block 2049, Block 2050, Block 2051,···, Block 4095

Address input restriction for the Multi Page Program with Data Cache operation

There are following restrictions in using Multi Page Program with Data Cache;

(Restriction)
District0 and District1 should be selected within the same chip.
Maximum one block should be selected from each District.
Same page address (PA0 to PA5) within two districts has to be selected.
For example;
(80) [District 0, Page Address 0x00000] (11) (80) [District 1, Page Address 0x20000] (15 or 10)
(80) [District 0, Page Address 0x00001] (11) (80) [District 1, Page Address 0x20001] (15 or 10)

(Acceptance)
There is no order limitation of the District for the address input.
For example, following operation is accepted;
(80) [District 0] (11) (80) [District 1] (15 or 10)
(80) [District 1] (11) (80) [District 0] (15 or 10)

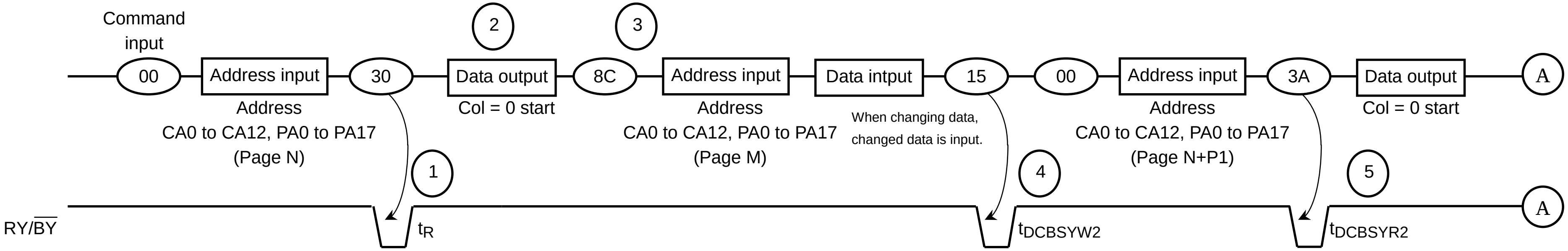
It requires no mutual address relation between the selected blocks from each District.

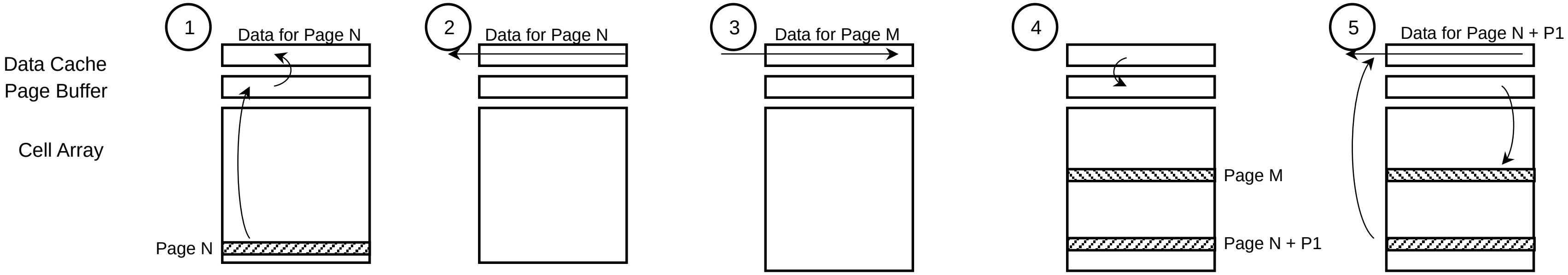
Operating restriction during the Multi Page Program with Data Cache operation

(Restriction)
The operation has to be terminated with "10h" command.
Once the operation is started, no commands other than the commands shown in the timing diagram is allowed to be input except for Status Read command and reset command

Page Copy (2)

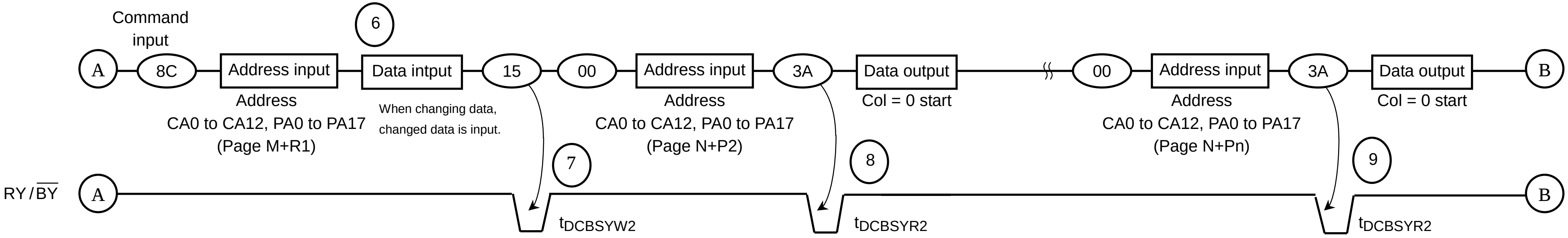
By using Page Copy (2), data in a page can be copied to another page after the data has been read out. When the block address changes (increments) this sequenced has to be started from the beginning.

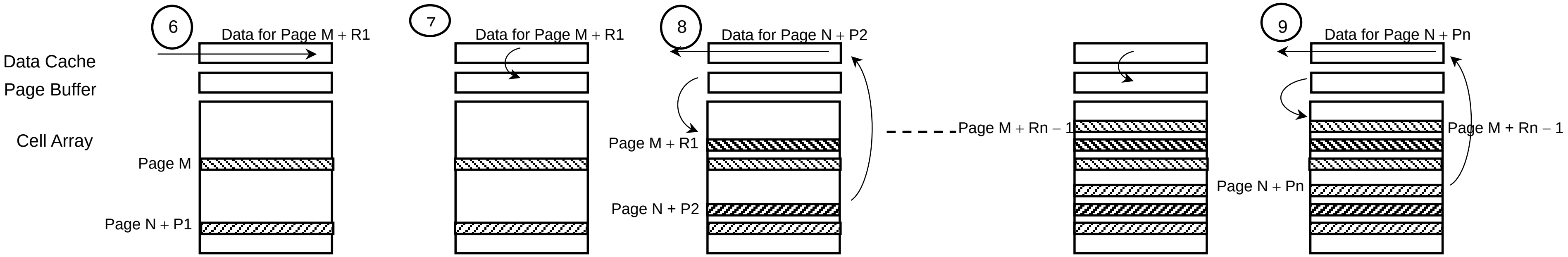




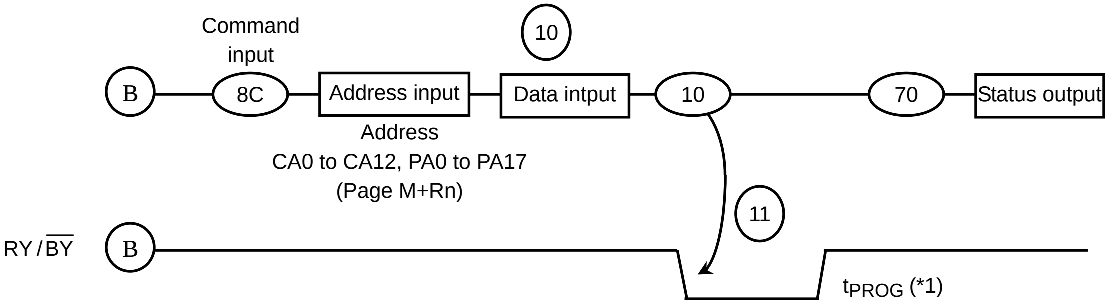
Page Copy (2) operation is as following.

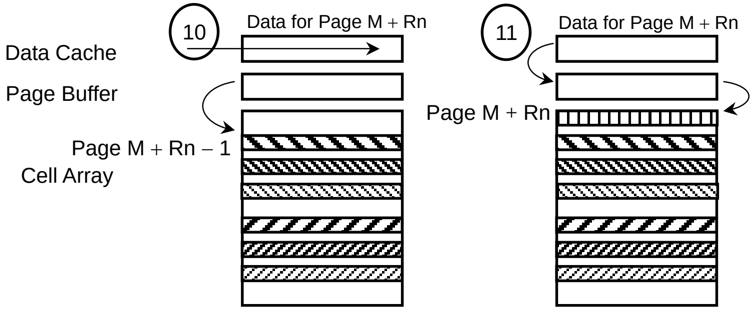
1 Data for Page N is transferred to the Data Cache.
2 Data for Page N is read out.
3 Copy Page address M is input and if the data needs to be changed, changed data is input.
4 Data Cache for Page M is transferred to the Page Buffer.
5 After the Ready state, Data for Page N + P1 is output from the Data Cache while the data of Page M is being programmed.





6 Copy Page address (M + R1) is input and if the data needs to be changed, changed data is input.
7 After programming of page M is completed, Data Cache for Page M + R1 is transferred to the Page Buffer.
8 By the 15h command, the data in the Page Buffer is programmed to Page M + R1. Data for Page N + P2 is transferred to the Data cache.
9 The data in the Page Buffer is programmed to Page M + Rn − 1. Data for Page N + Pn is transferred to the Data Cache.





10 Copy Page address (M + Rn) is input and if the data needs to be changed, changed data is input.
11 By issuing the 10h command, the data in the Page Buffer is programmed to Page M + Rn.

(*1) Since the last page programming by the 10h command is initiated after the previous cache program, the t_{PROG} here will be expected as the following,
$t_{PROG} = t_{PROG}$ of the last page + tPROG of the previous page − (command input cycle + address input cycle + data output/input cycle time of the last page)

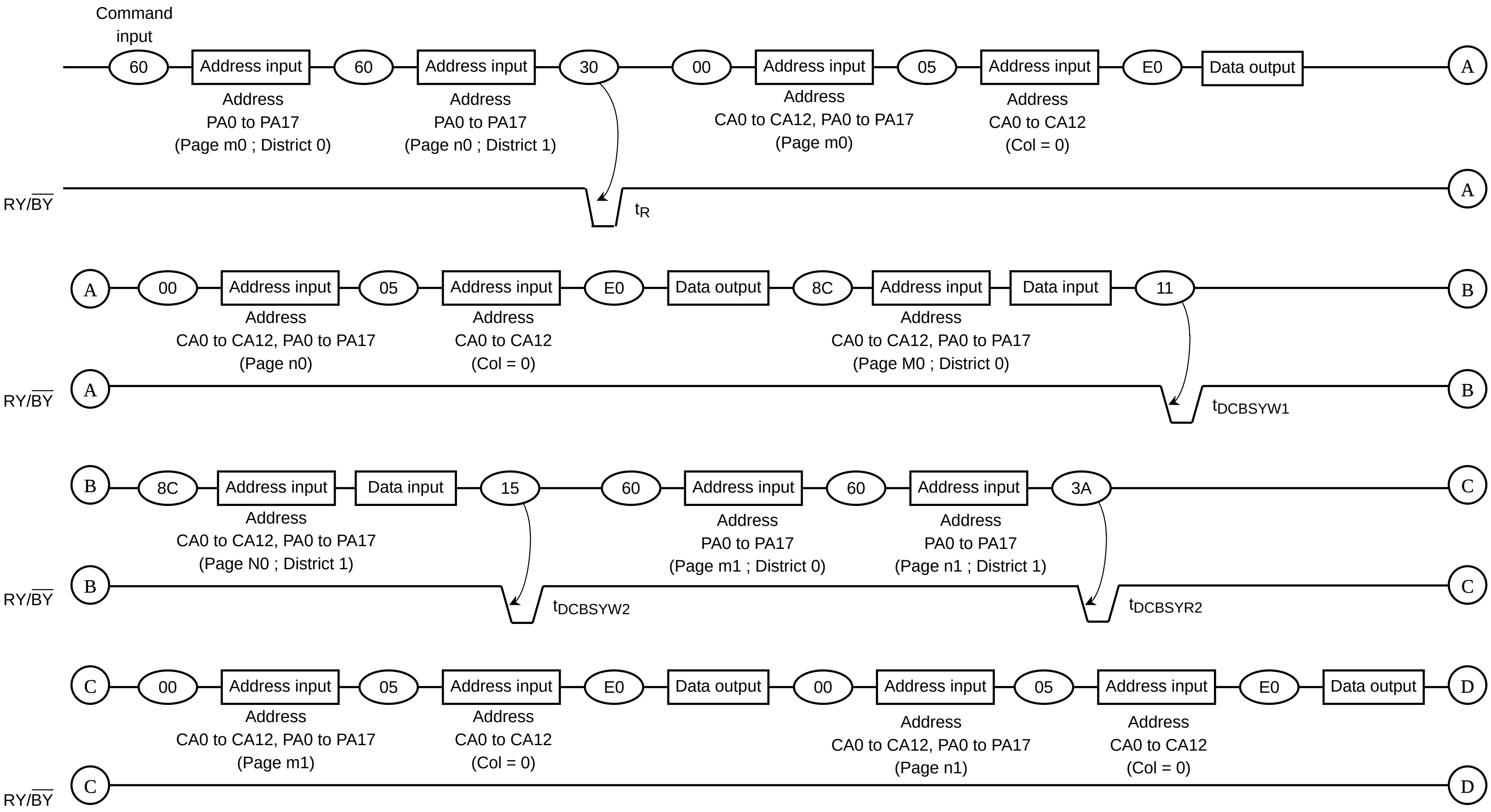
NOTE) This operation needs to be executed within District-0 (Block 0 − 2047) or District-1 (Block 2048 − 4095).

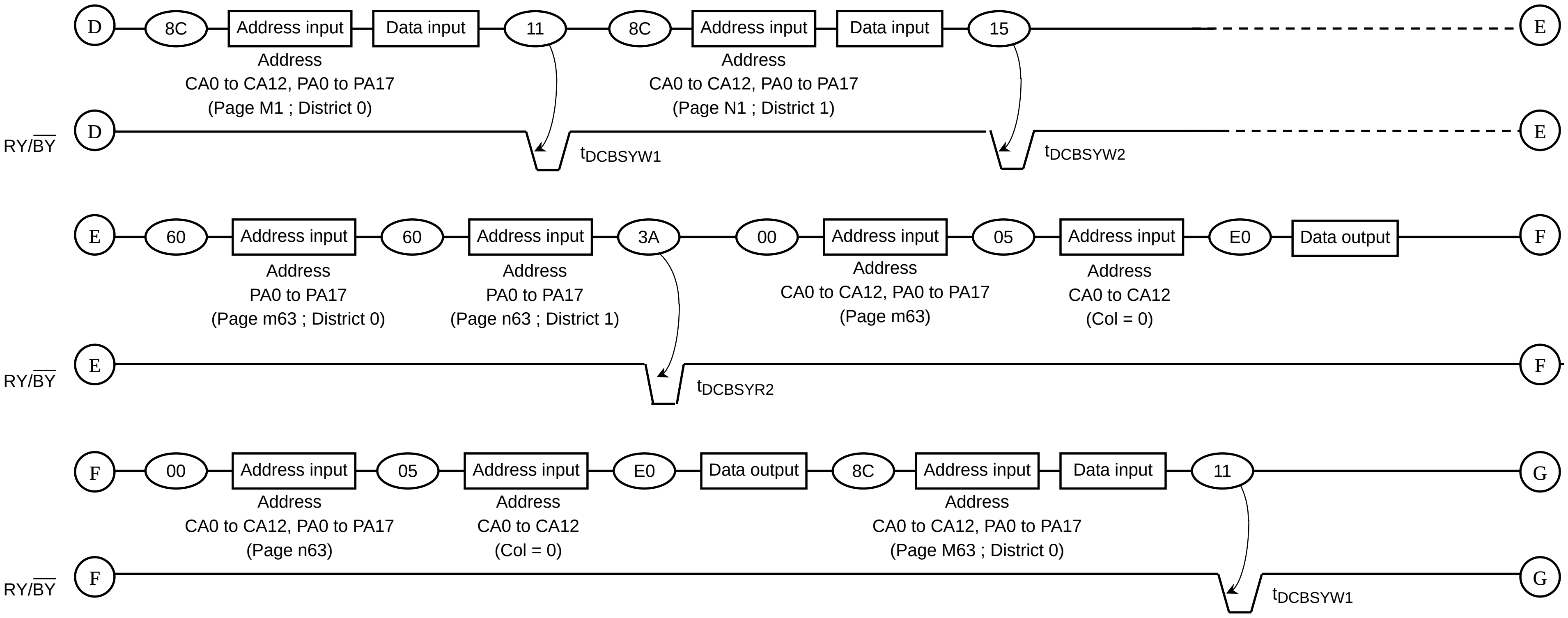
Data input is required only if previous data output needs to be altered.
If the data has to be changed, locate the desired address with the column and page address input after the 8Ch command, and change only the data that needs be changed.
If the data does not have to be changed, data input cycles are not required.

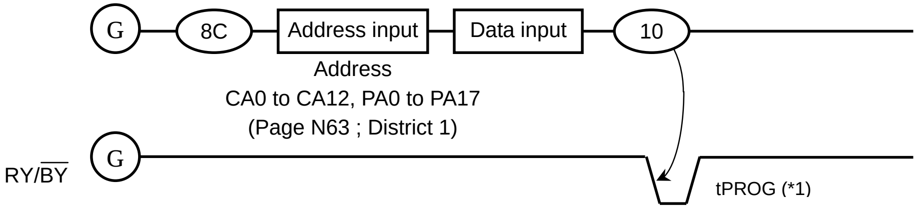
Make sure $\overline{WP}$ is held to High level when Page Copy (2) operation is performed.
Also make sure the Page Copy operation is terminated with 8Ch-10h command sequence

Multi Page Copy (2)

By using Multi Page Copy (2), data in two pages can be copied to another pages after the data has been read out.
When the each block address changes (increments) this sequenced has to be started from the beginning.
Same page address (PA0 to PA5) within two districts has to be selected.







(*1) t_{PROG}: Since the last page programming by 10h command is initiated after the previous cache program, the t_{PROG*} during cache programming is given by the following equation.

t_{PROG} = t_{PROG} of the last page + t_{PROG} of the previous page-A
A = (command input cycle + address input cycle + data output/input cycle time of the last page)
If "A" exceeds the t_{PROG} of previous page, t_{PROG} of the last page is t_{PROG} max.

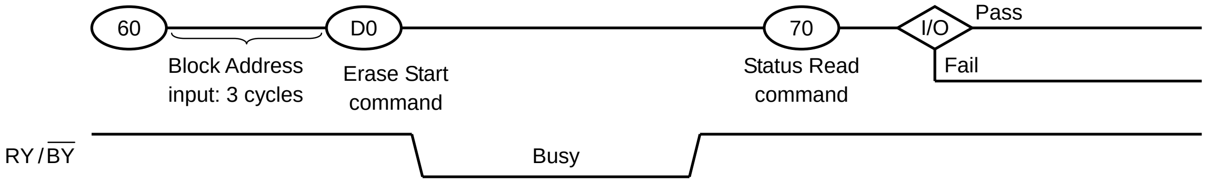
Note)
This operation needs to be executed within each District.

Data input is required only if previous data output needs to be altered.
If the data has to be changed, locate the desired address with the column and page address input after the 8Ch command, and change only the data that needs be changed.
If the data does not have to be changed, data input cycles are not required.

Make sure $\overline{\text{WP}}$ is held to High level when Multi Page Copy (2) operation is performed.
Also make sure the Multi Page Copy operation is terminated with 8Ch-10h command sequence

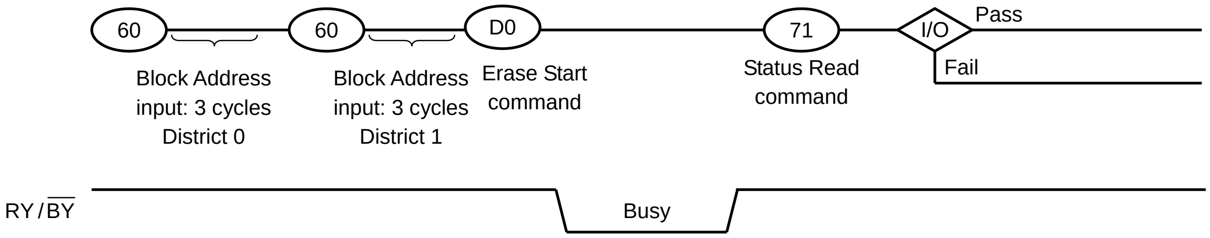
Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command "D0h" which follows the Erase Setup command "60h". This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



Multi Block Erase

The Multi Block Erase operation starts by selecting two block addresses before D0h command as in below diagram. The device automatically executes the Erase and Verify operations and the result can be monitored by checking the status by 71h status read command. For details on 71h status read command, refer to section "Multi Page Program with Data Cache".



Internal addressing in relation with the Districts

To use Multi Block Erase operation, the internal addressing should be considered in relation with the District.

- The device contains two chips of NAND EEPROM.
- Each internal chip consists from 2 Districts.
- Each District consists from 2048 erase blocks.
- The allocation rule is follows.
  District 0: Block 0, Block 1, Block 2, Block 3,⋯, Block 2047
  District 1: Block 2048, Block 2049, Block 2050, Block 2051,⋯, Block 4095

Address input restriction for the Multi Block Erase

There are following restrictions in using Multi Block Erase

(Restriction)
District0 and District1 should be selected within the same chip.
Maximum one block should be selected from each District.
For example;
(60) [District 0] (60) [District 1] (D0)

(Acceptance)
There is no order limitation of the District for the address input.
For example, following operation is accepted;
(60) [District 1] (60) [District 0] (D0)

It requires no mutual address relation between the selected blocks from each District.

Make sure to terminate the operation with D0h command. If the operation needs to be terminated before D0h command input, input the FFh reset command to terminate the operation.

ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

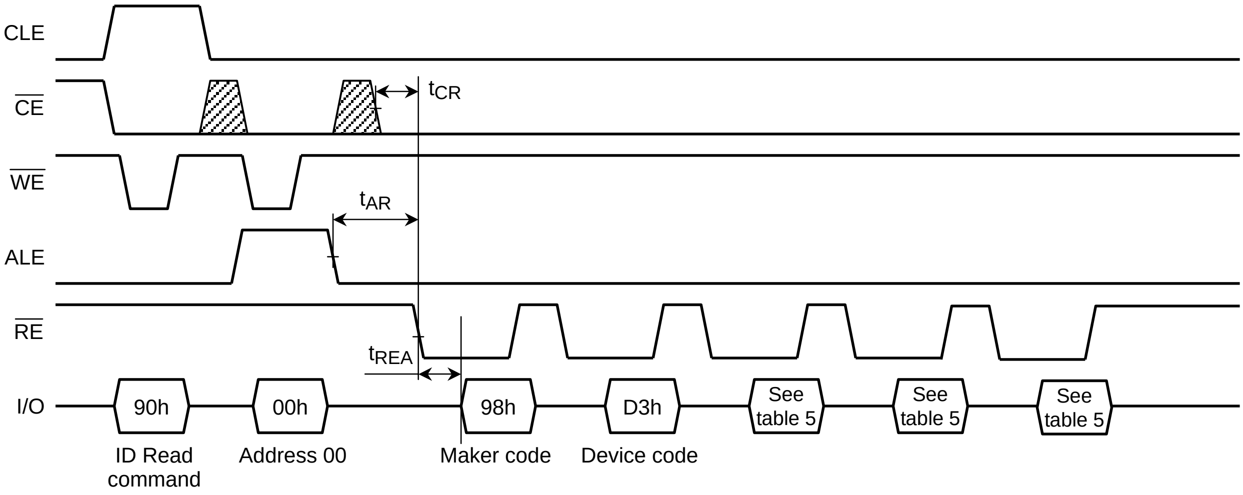


Table 5. Code table

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98h
2nd Data	Device Code	1	1	0	1	0	0	1	1	D3h
3rd Data	Chip Number, Cell Type	1	0	0	1	0	0	0	0	See table
4th Data	Page Size, Block Size, Redundant Size, Organization	1	0	1	0	1	0	1	0	See table
5th Data	Extended Block	—	1	1	0	0	1	0	0	See table

3rd Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 level cell					0	0		
	4 level cell					0	1		
	8 level cell					1	0		
	16 level cell					1	1		
Reserved		0 or 1	0	0 or 1	0 or 1				

4th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Page Size (without redundant area)	1 KB 2 KB 4 KB 8 KB							0 0 1 1	0 1 0 1
Block Size (without redundant area)	64 KB 128 KB 256 KB 512 KB			0 0 1 1	0 1 0 1				
Redundant area size	8byte/512byte 16byte/512byte 218byte/4096byte Reserved					0 0 1 1	0 1 0 1		
Organization	×8		0						
Reserved		0 or 1							

5th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Extended Block	Not available Available							0 1	
Reserved		0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1		0 or 1

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass /fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using $\overline{\text{RE}}$ after a “70h” command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status.

The resulting information is outlined in Table 6.

Table 6. Status output table

	Definition	Page Program Block Erase	Cache Program	Read Cache Read
I/O1	Chip Status1 Pass: 0 Fail: 1	Pass/Fail	Pass/Fail	Invalid
I/O2	Chip Status 2 Pass: 0 Fail: 1	Invalid	Pass/Fail	Invalid
I/O3	Not Used	0	0	0
I/O4	Not Used	0	0	0
I/O5	Not Used	0	0	0
I/O6	Page Buffer Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O7	Data Cache Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O8	Write Protect Not Protected :1 Protected: 0	Write Protect	Write Protect	Write Protect

The Pass/Fail status on I/O1 and I/O2 is only valid during a Program/Erase operation when the device is in the Ready state.

Chip Status 1:

During a Auto Page Program or Auto Block Erase operation this bit indicates the pass/fail result.

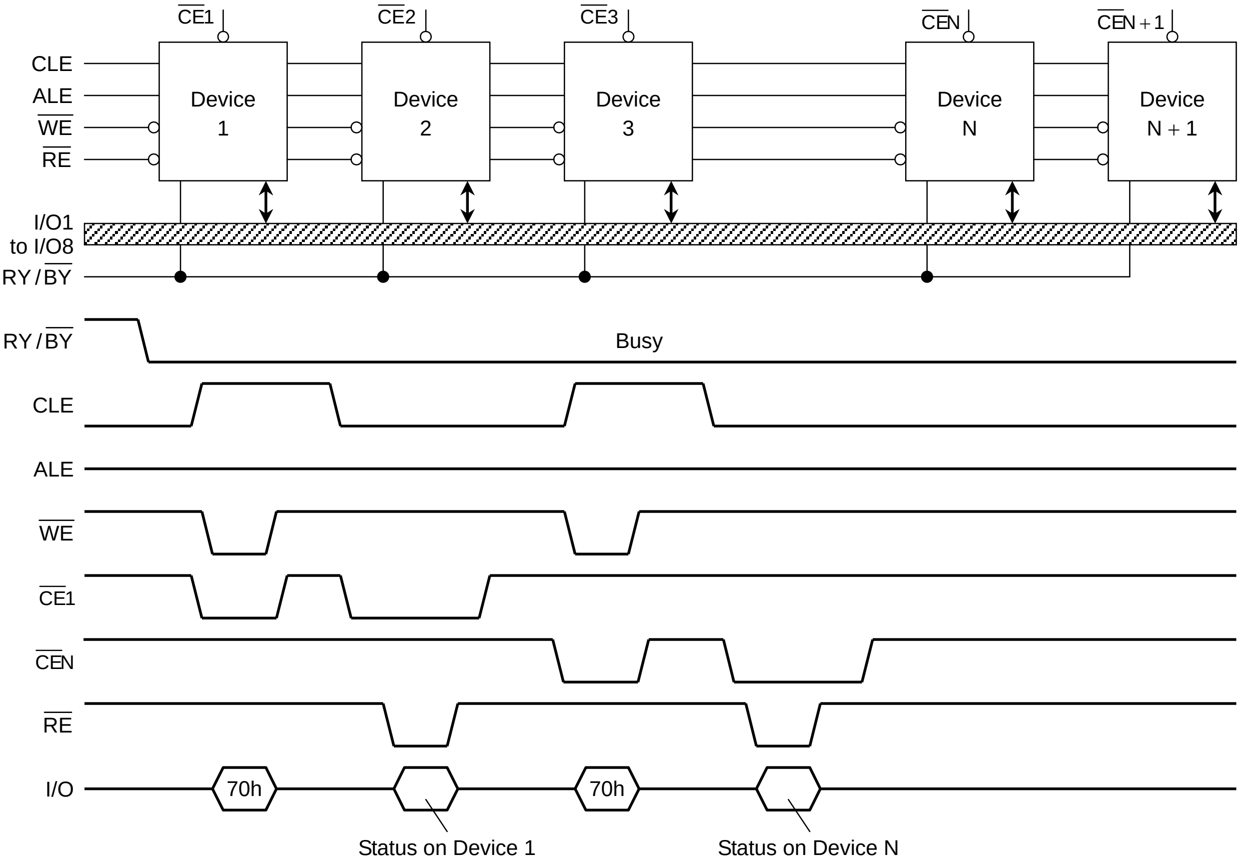
During a Auto Page Programming with Data Cache operation, this bit shows the pass/fail results of the current page program operation, and therefore this bit is only valid when I/O6 shows the Ready state.

Chip Status 2:

This bit shows the pass/fail result of the previous page program operation during Auto Page Programming with Data Cache. This status is valid when I/O7 shows the Ready State.

The status output on the I/O6 is the same as that of I/O7 if the command input just before the 70h is not 15h or 31h.

An application example with multiple devices is shown in the figure below.



System Design Note: If the RY / BY pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

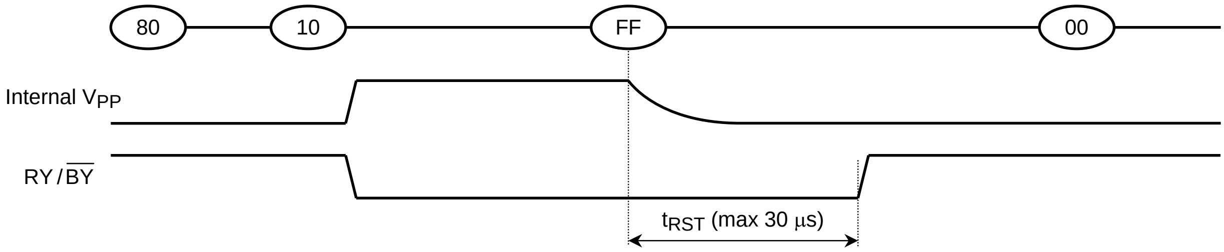
Reset

The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 volt and the device enters the Wait state.

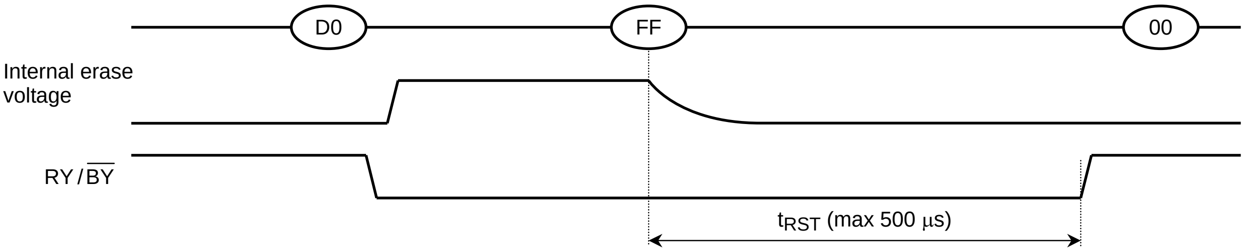
Reset during a Cache Program/Page Copy may not just stop the most recent page program but it may also stop the previous program to a page depending on when the FF reset is input.

The response to a “FFh” Reset command input during the various device operations is as follows:

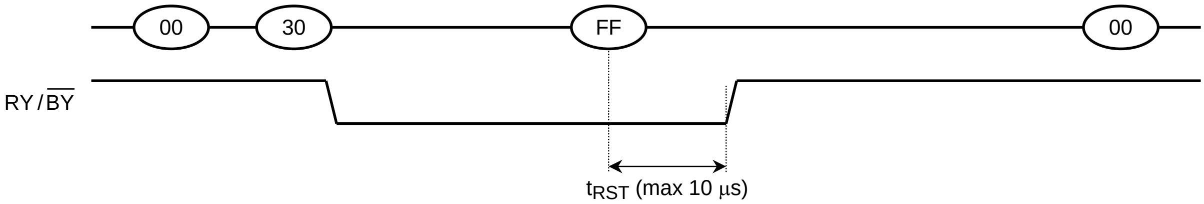
When a Reset (FFh) command is input during programming



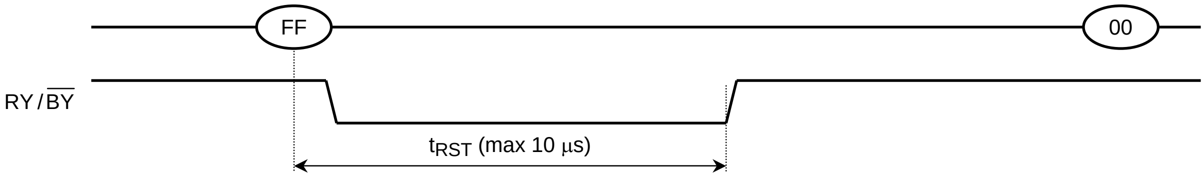
When a Reset (FFh) command is input during erasing



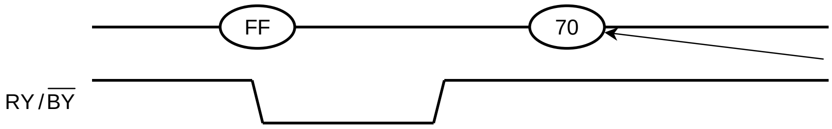
When a Reset (FFh) command is input during Read operation



When a Reset (FFh) command is input during Ready

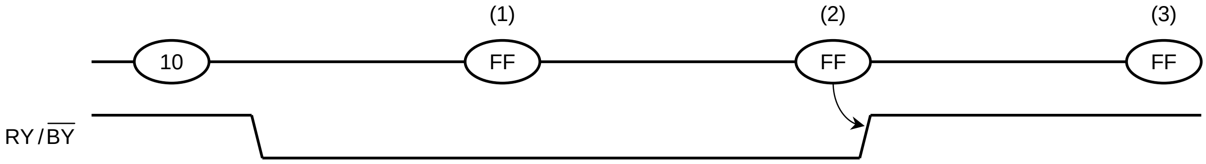


When a Status Read command (70h) is input after a Reset



I/O status: Pass/Fail → Pass
: Ready/Busy → Ready

When two or more Reset commands are input in succession



The second FF command is invalid, but the third FF command is valid.

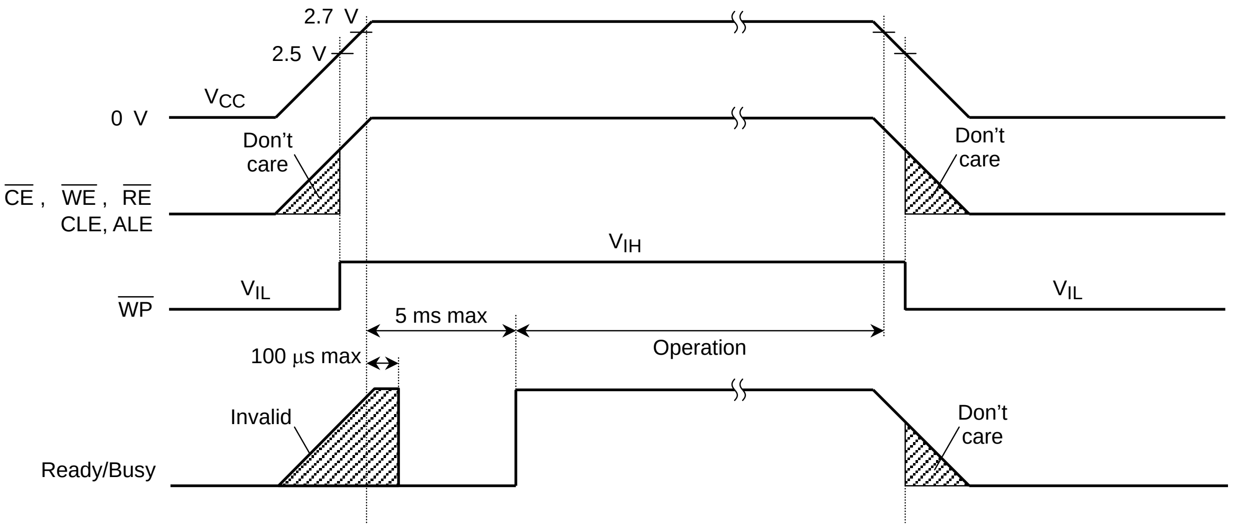
APPLICATION NOTES AND COMMENTS

(1) Power-on/off sequence:

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

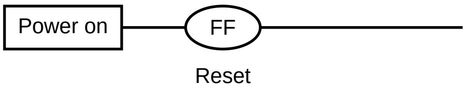
The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h(71h).

The $\overline{\text{WP}}$ signal is useful for protecting against data corruption at power-on/off.



(2) Power-on Reset

The device goes into automatic self initialization during power on if PSL is tied either to GND or NU. During the initialization process, the device consumes a maximum current of 30 mA (I_{CCO0}). If PSL is tied to VCC, the device will not complete its self initialization during power on and will not consume I_{CCO0}, and completes the initialization process with the first Reset command input after power on. During the first FFh reset Busy period, the device consumes a maximum current of 30 mA (I_{CCO0}). In either case (PSL = GND/ NU or V_{CC}), the following sequence is necessary because some input signals may not be stable at power-on.



(3) Prohibition of unspecified commands

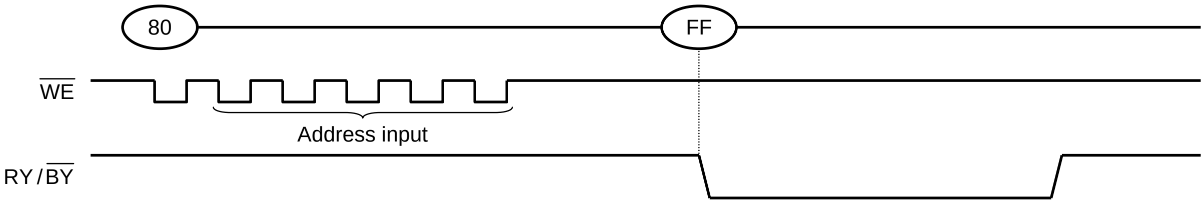
The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(4) Restriction of commands while in the Busy state

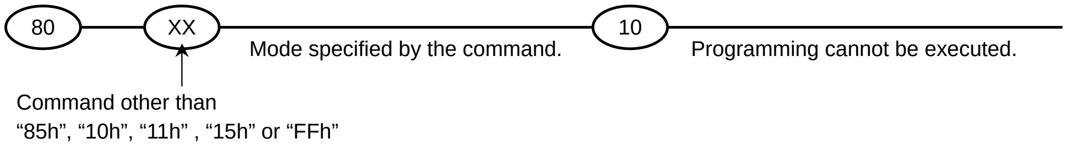
During the Busy state, do not input any command except 70h(71h) and FFh.

(5) Acceptable commands after Serial Input command “80h”

Once the Serial Input command “80h” has been input, do not input any command other than the Column Address Change in Serial Data Input command “85h”, Auto Program command “10h”, Multi Page Program command “11h”, Auto Program with Data Cache Command “15h”, or the Reset command “FFh”.



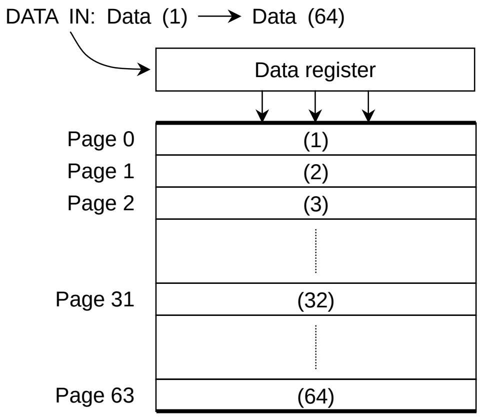
If a command other than “85h”, “10h” , “11h” , “15h” or “FFh” is input, the Program operation is not performed and the device operation is set to the mode which the input command specifies.



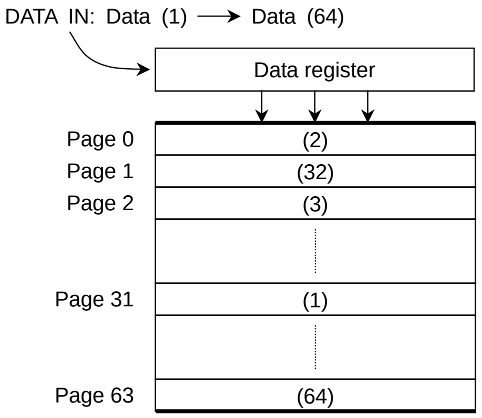
(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

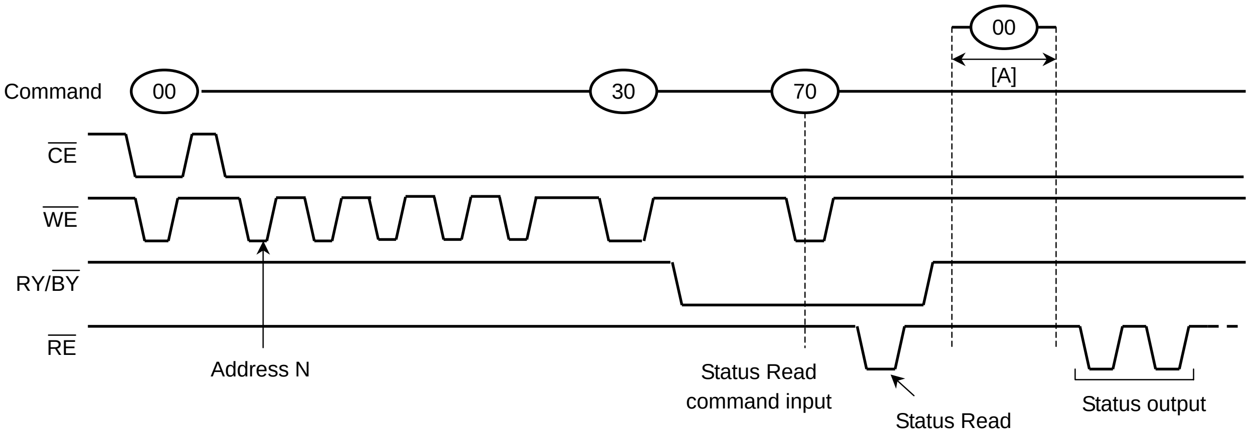
From the LSB page to MSB page



Ex.) Random page program (Prohibition)

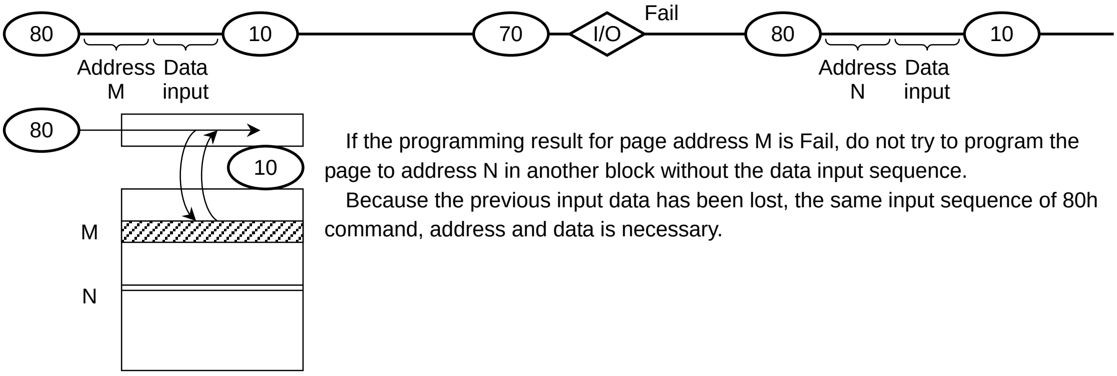


(7) Status Read during a Read operation



The device status can be read out by inputting the Status Read command “70h” in Read mode. Once the device has been set to Status Read mode by a “70h” command, the device will not return to Read mode unless the Read command “00h” is input during [A]. If the Read command “00h” is input during [A], Status Read mode is reset, and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

(8) Auto programming failure

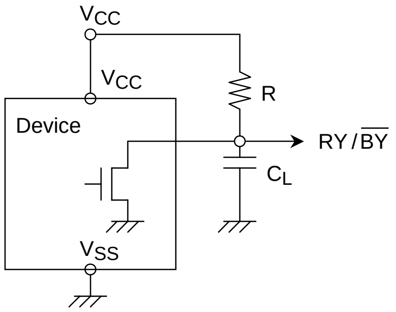


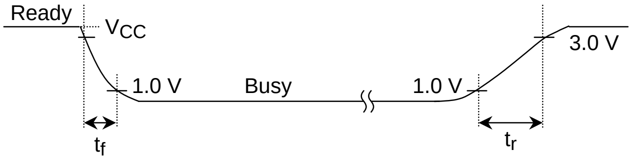
If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence.

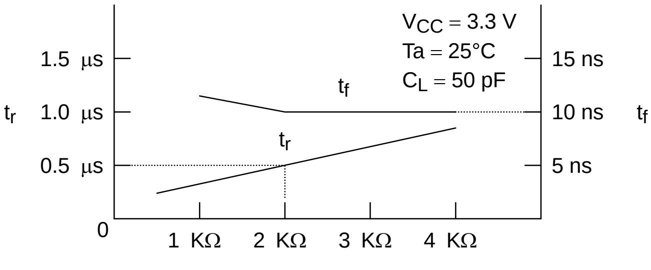
Because the previous input data has been lost, the same input sequence of 80h command, address and data is necessary.

(9) RY / $\overline{BY}$: termination for the Ready/Busy pin (RY / $\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY / $\overline{BY}$ buffer consists of an open drain circuit.





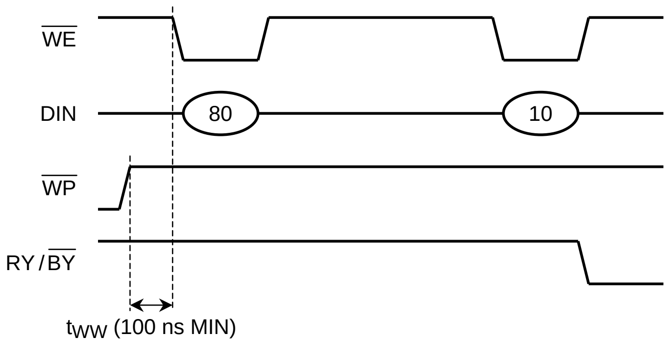


This data may vary from device to device. We recommend that you use this data as a reference when selecting a resistor value.

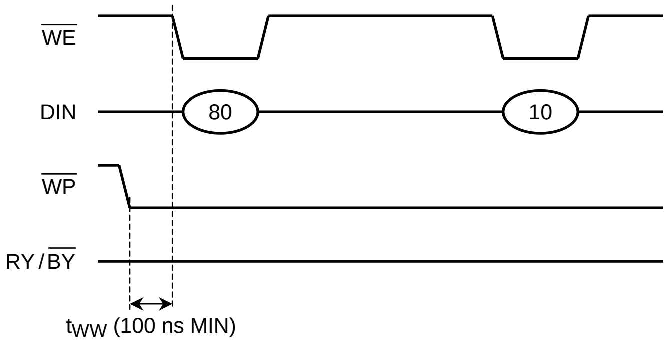
(10) Note regarding the $\overline{WP}$ signal

The Erase and Program operations are automatically reset when $\overline{WP}$ goes Low. The operations are enabled and disabled as follows:

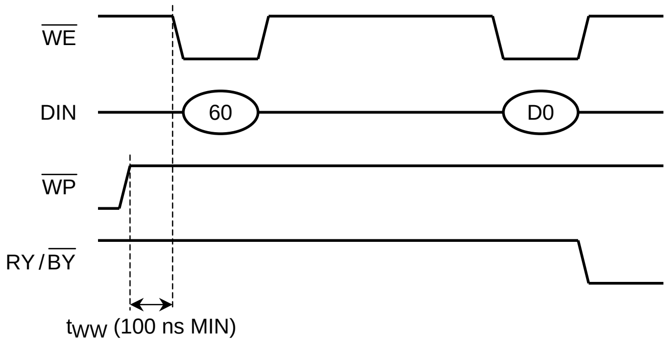
Enable Programming



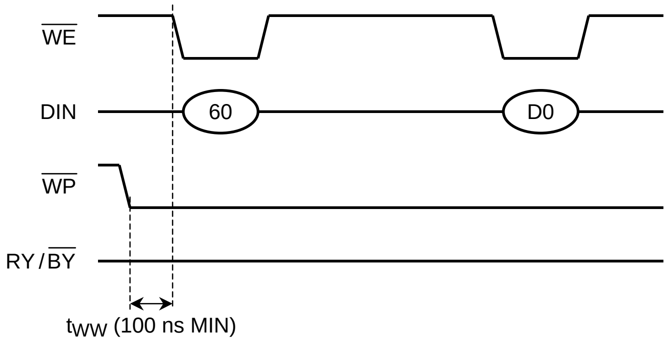
Disable Programming



Enable Erasing



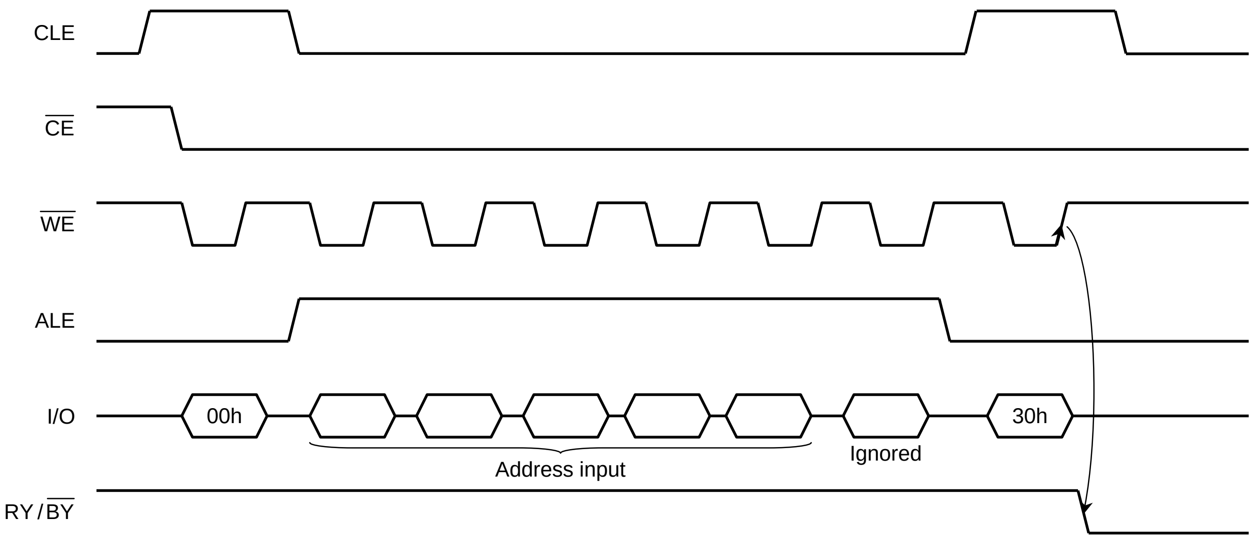
Disable Erasing



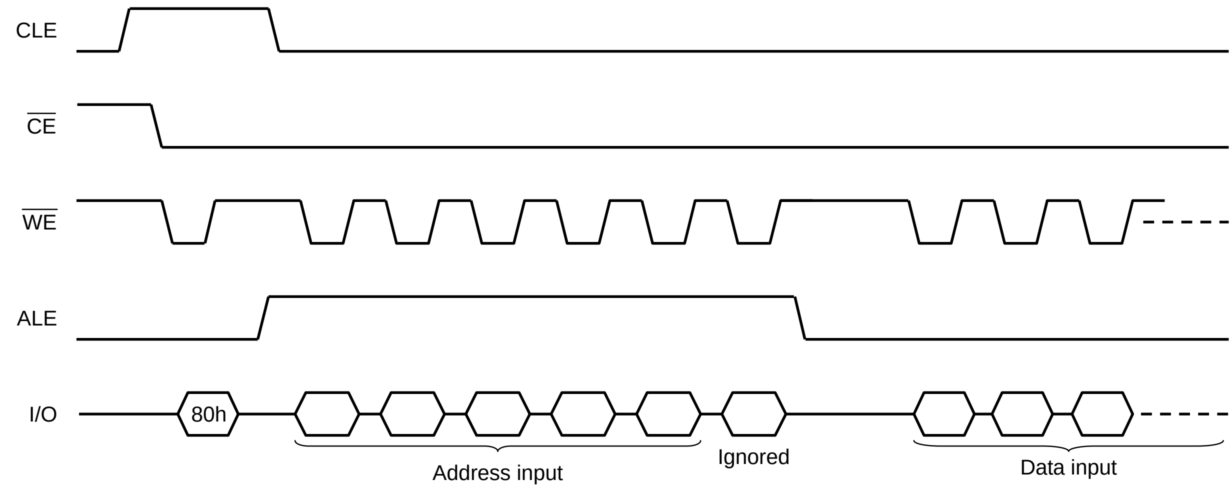
(11) When six address cycles are input

Although the device may read in a sixth address, it is ignored inside the chip.

Read operation

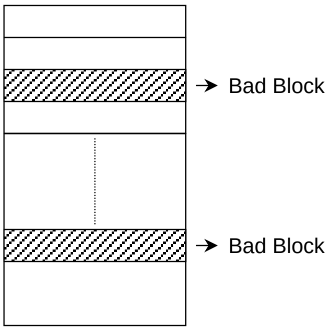


Program operation



(12) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



At the time of shipment, the bad block information is marked on each bad block. Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.

Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

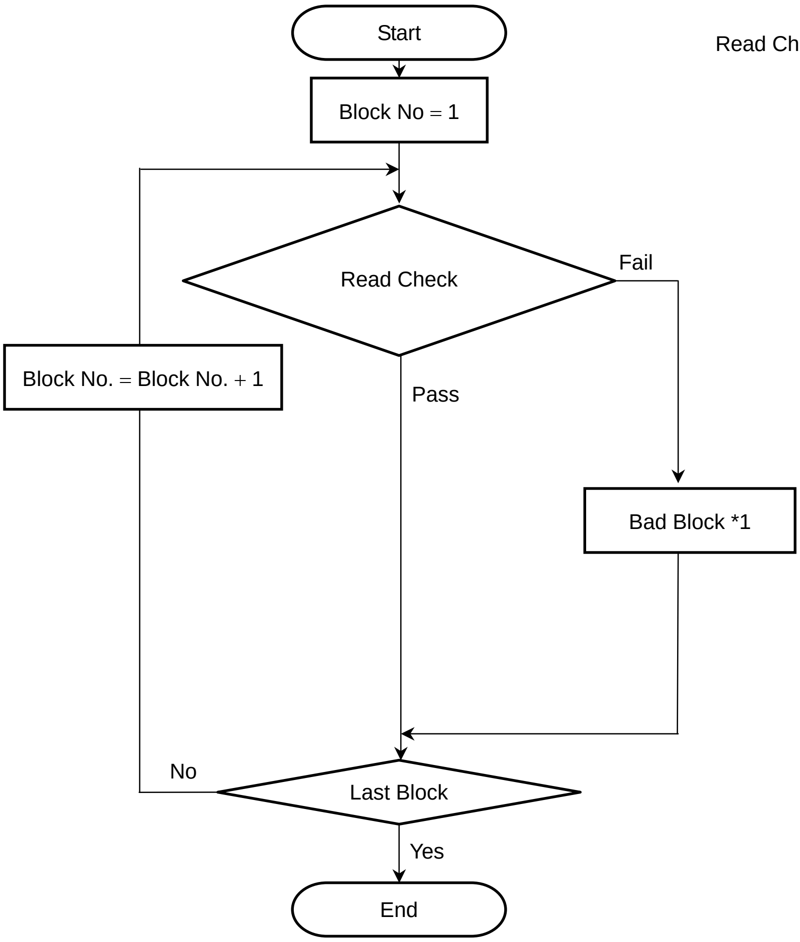
A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

The number of valid blocks over the device lifetime is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	8032	—	8192	Block

Bad Block Test Flow

Regarding invalid blocks, bad block mark is in either the 1st or the 2nd page.



Read Check: Read either column 0 or 4096 of the 1st page or the 2nd page of each block. If the data of the column is not FF (Hex), define the block as a bad block.

*1: No erase operation is allowed to detected bad blocks

(13) Failure phenomena for Program and Erase operations

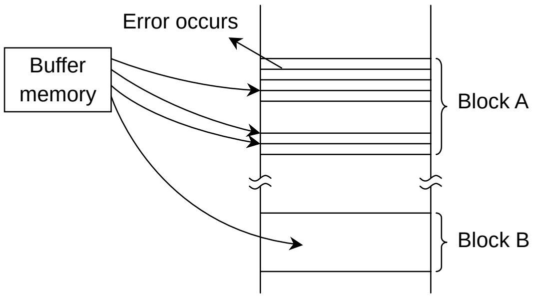
The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Single Bit	Programming Failure “1 to 0”	ECC

- ECC: Error Correction Code. 1 bit correction per 512Bytes is necessary.

- Block Replacement

Program



When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(14) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

(15) Reliability Guidance

This reliability guidance is intended to notify some guidance related to using NAND flash with 1bit ECC for each 512 bytes. For detailed reliability data, please refer to TOSHIBA's reliability note.
Although random bit errors may occur during use, it does not necessarily mean that a block is bad.
Generally, a block should be marked as bad when a program status failure or erase status failure is detected.
The other failure modes may be recovered by a block erase.
ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

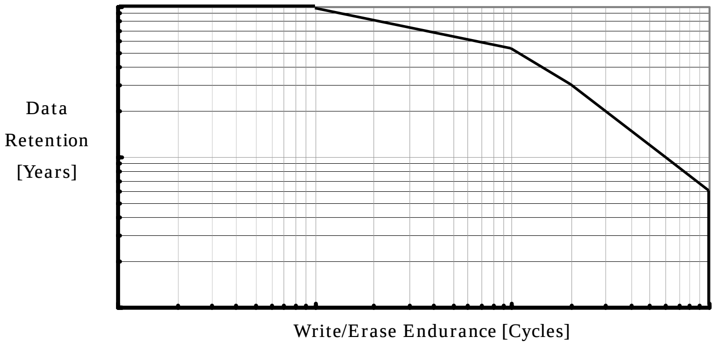
- **Write/Erase Endurance**

  Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

- **Data Retention**

  The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again.

  Here is the combined characteristics image of Write/Erase Endurance and Data Retention.



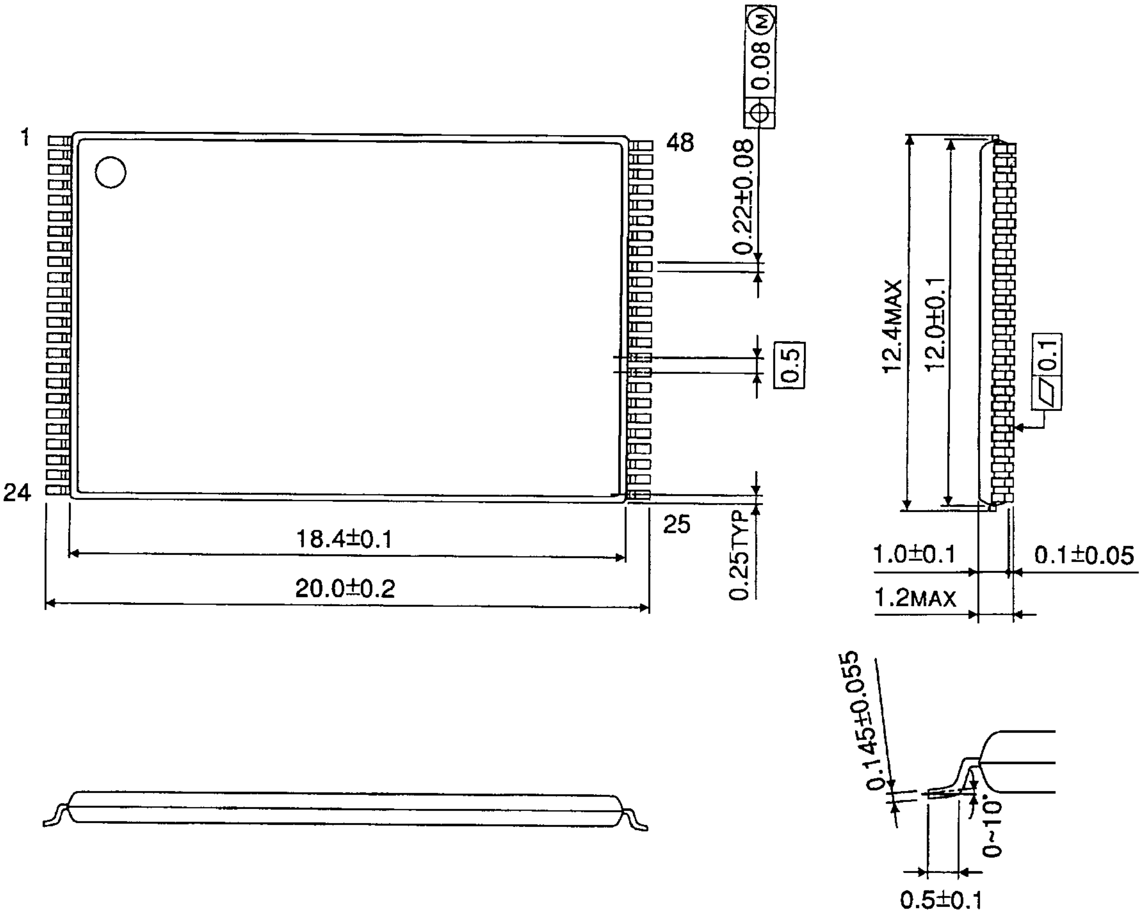
- **Read Disturb**

  A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

Package Dimensions

TSOP I 48-P-1220-0.50

Unit : mm



Weight: 0.53 g (typ.)

Revision History

Date	Rev.	Description
2008-02-01	1.00	Original version

RESTRICTIONS ON PRODUCT USE

060915EBA_R6

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